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Switching Activity Reduction Technique In Soc Testing

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Abstract- **This paper discusses the generation Pseudo Random number generation using Low Power Linear Feedback Shift Resister (LFSR) which is more suitable for Built-In-Test (BIT) structures used for testing of VLSI circuits. BIT is a design for testability (DFT) technique in which testing is carried out using built in hardware features. Since testing is built into the hardware, it is faster and efficient. The proposed test pattern generator reduces the switching activity among the test patterns.**

Keywords — **LFSR, BIST, DFT, Power Dissipation, Booth Multiplier, Array Multiplier, Test Patterns.**

I. INTRODUCTION

Power dissipation is a challenging problem for system-on-chips (SOCs) design and test. The dynamic power of a circuit in which all the transistors switch exactly once per clock cycle will be $1/2CV^2$ F , if C is the switched capacitance, V is the supply voltage, and F is the clock frequency. However, most of the transistors in a circuit rarely switch from most input changes. Hence, a constant called the activity factor ($0 \leq A \leq 1$) is used to model the average switching activity in the circuit. Using A, the dynamic power of a circuit composed of CMOS transistors (Fig.1) can be estimated as:

$$p= a\, cv^2 f$$

The importance of this equation points towards the fundamental mechanisms of reducing switching power. Fig.2 shows that one scheme is by reducing the activity factor A. The question here is: "how to achieve the same functionality by switching only a minimal number of transistors?" Techniques to do this span several design hierarchy levels, right from the synthesis level, where, for example, we can encode states so that the most frequent transitions occur with minimal bit switches, to the algorithmic level, where, for example, changing the sorting algorithm from insertion sort to quick sort, will asymptotically reduce the resulting switching activity. The second fundamental scheme is to reduce the load capacitance C. This can be done by using small transistors with low capacitances in non-critical parts of the circuit. Reducing the frequency of operation F will cause a linear reduction in dynamic power, but reducing the supply voltage VDD will cause a quadratic reduction. In the following sections we discuss some of the established and effective mechanisms for dynamic power reduction.

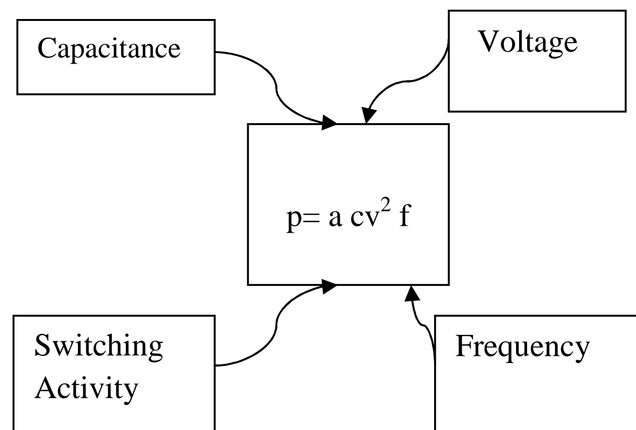

Fig.1. Estimation of Dynamic power of a circuit composed of CMOS transistor.

charging and discharging circuit nodes. C represents the node capacitance and N is the switching activity i.e., the number of gate output transitions per clock cycle(also known as transition density)is the energy involved in charging or discharging a circuit with node capacitance C and is the average number of times per second that the node switches. The second term in (1) represents the power dissipation due to current flowing directly from the supply to ground. During this period that the pull-up and pull-down networks of the CMOS gate are both conducting when the output switches. This current is often called short circuit current. The factor represents the quantity of charge carried by the short circuit current per transition. The third term in (1) is related to the static power dissipation due to leakage current. The transistor source and drain diffusions in a MOS device from parasitic diodes with bulk regions. Reverse bias current in these diodes dissipate power.

The low power test pattern generator presented in [3] is based on cellular automata, reduces the test power in combinational circuits. Another low-power test pattern generator based on a modified LFSR is proposed in [4]. This scheme reduces the power in circuit under test (CUT) in general and clock tree in particular. A low-power BIST for data path architecture, built around multiplier-accumulator pairs, is proposed in [5]. The drawback is that these techniques are circuit-dependent, implying that non-detecting subsequences must be determined for each circuit test sequence. A low power BIST based on state correlation analysis proposed in [6].Modifying the LFSR, by adding weights to tune the

pseudorandom vectors for various probabilities, decreases energy consumption and increases fault coverage [7] [8]. A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [9]. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power.. Test vector inhibiting techniques [11] filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR. These architectures apply the minimum number of test vectors required to attain the desired fault coverage and therefore reduce power.

II. BIST ARCHITECTURE

Built-in Test (BIT) is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, thereby reducing dependence on external automated test equipment (ATE).

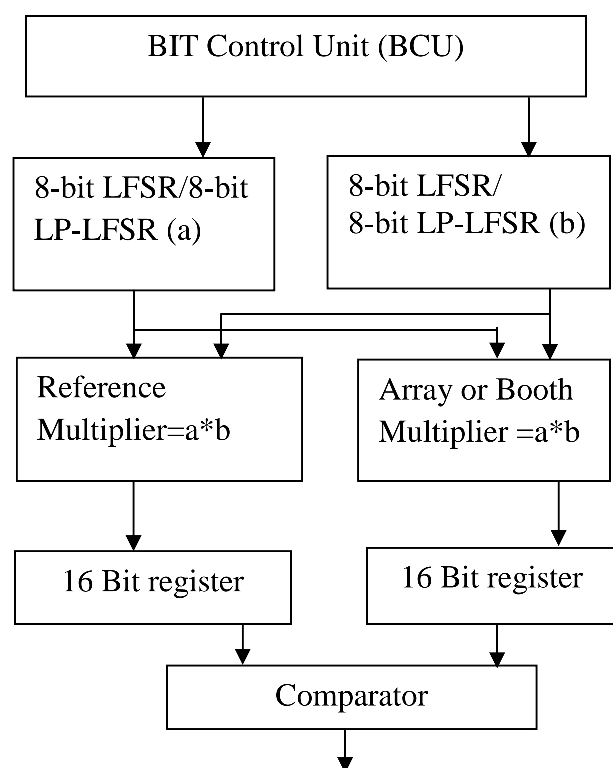

Fig 2: BIST Architecture

The components of BIST architecture is given below.

1. Circuit under test : It is the circuit to be tested. It can be either combinational, sequential or memory.

2. Test pattern generator : It generates test patterns for CUT. It is generally a LFSR or ATPG.

3.1Parallel-In-Parallel-Out: It is designed for signature analysis, which is a technique for data compression.

4. Comparator: It compares the value of primary output with the expected output.

5. BIST control unit (BCU): It controls the test execution and manages all the components of a BIST circuit.

III. MULTIPLIER

Multipliers have large area, long latency and consume considerable power. Reduction of power consumption makes a device reliable. Therefore, low power multipliers with high clock frequencies play an important role in today's digital signal processing. Digital signal processing (DSP) is the technology at the heart of the next generation of personal mobile communication systems. Most DSP systems incorporate a multiplication unit to implement algorithms such as convolution and filtering. Multiplications are basic arithmetic operations used virtually in all applications involving digital signal processing. Multiplication can be considered as a series of repeated additions. Design of portable battery operated multimedia devices requires energy efficient multiplication circuits.

Types of Multiplier

Multipliers are classified by the format in which words are accessed namely:

A. Array Multiplier
B. Booth Multiplier

A. Introduction to Array Multiplier: The Fig.3 shows Array Multiplier, in each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits.

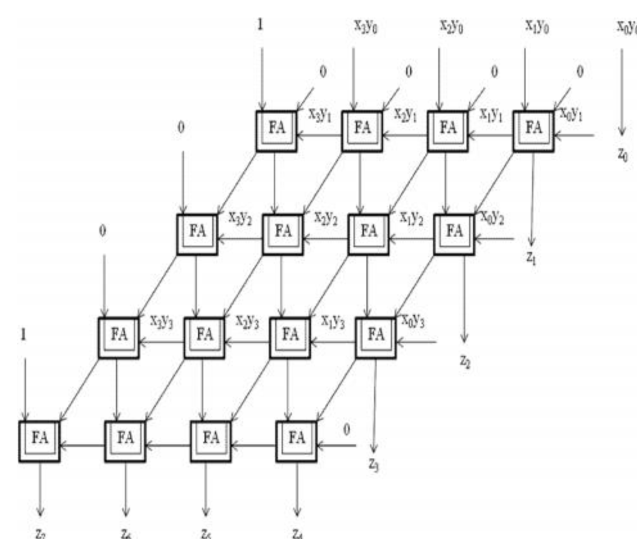

Fig 3: Array Multiplier

B. Booth Multiplier: The Fig.4 shows the booth multiplier which performs both Signed and Unsigned operations. The main objective of designing the booth multiplier is to perform the partial products to reduce the delay and to increase the speed of the circuit. In this it also reduce the area of the chip used so the power consumption is also reduced in this circuit. The main operation of the booth decoder is to convert the given input to the equivalent booth value. So it contains more number of zeros.

The maximum delay time in the tree type binary multiplying circuit can be determined by the sum of a time in which partial products are formed from the output of the booth decoder having a multiplier provided and a multiplicand, and a time in which the thus formed partial products are added.

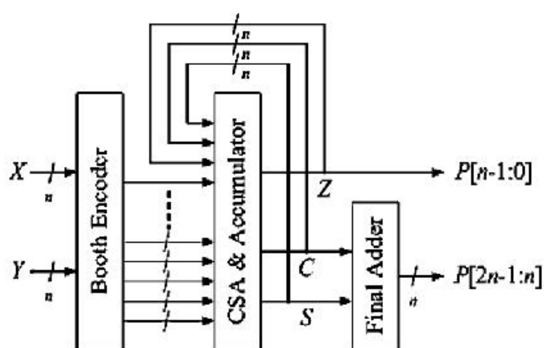

Fig 4: Booth Multiplier for Signed and Unsigned operation

By combining the Booth decoders with the partial product generating circuits, the partial products of (m+1) bits should be generated from m multiplicand.

IV. PRIOR WORK

A. Linear Feedback Shift Register (LFSR)

Linear Feedback Shift Register is a circuit consisting of flip-flops connected in series with each other. The output of one flip-flop is connected to the input of the next flip flop and so on. The feedback polynomial which is also known as the characteristic polynomial is used to determine the feedback taps which in turn determines the length of the random pattern generation.

An example below in Fig.5. is used to illustrate the correlation between the LFSR, its characteristic polynomial and matrix theory. In the circuit the feedback taps are shown to be from the output of the 3rd and 1st register.

These taps are indicative of the generator polynomial. Using the matrix theory the companion matrix required for relating the present to the next state is depicted. The actual sequence of the LFSR is represented as BT1, BT2, BT3… where B is the seed vector. The determinant of the T matrix is called the characteristic polynomial and the generator polynomial is the inverse of the characteristic polynomial.

The increased power consumption by the device in the manufacturing test environment therefore can in most cases exceed the maximum power consumption specification of the IC resulting in un-repairable device failures begins with a pattern generated using a conventional LFSR causing significant loss of yield. Earlier Techniques for reducing the power dissipation during testing are

1. Another technique was proposed in [3] that is Low transition LFSR for BIST applications. This reduces the average and peak power of circuit during testing.
2. In [4], a Fault model& ATPG algorithm is chosen first, and then test patterns are generated to achieve the desired fault coverage.
3. Proposed a Low power test pattern generation for sequential circuit in [5]. In this paper redundancy is introduced during testing. This will reduces the power consumption without affecting the fault coverage.

Standard LFSR:

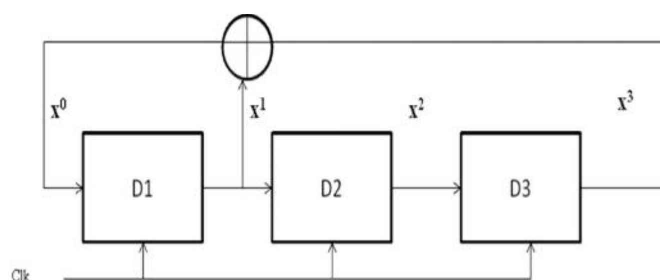

Fig 5. 3-bit LFSR Architecture (tap1)

A Linear Feedback Shift Register (LFSR) is a type of pseudorandom number generator. To illustrate an LFSR operation, consider a register that is 3-bits wide.

Start by loading it with an initial seed value. Shift it to the right, and XOR the bit at the output of the last flip-flop and first flip-flop. Then the output of XOR gate is fed to the input of first flip-flop. The seed to be 100

The characteristic polynomial in the general case of an n-bit LFSR to be primitive polynomial it should

- Result in a remainder not equal to 1 for all n $L< q^n -1$
- Remainder of 1 for $L= q^n -1$

Where n=higher order in Characteristic Equation (C.E)

Where q =2 (0 or 1)

Here n=3

$L= q^n -1$

For L=3; it result in remainder not equal to 1

For L=4; it result in remainder not equal to 1

For L=5; it result in remainder not equal to 1

For L=6; it result in remainder not equal to 1

Therefore first condition is satisfied i.e remainder not equal to 1 for all n $L< q^n -1$ i.e L=3,4,5,6.

For L=7 result in remainder equal to 1

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Therefore second condition is satisfied i.e. remainder equal to 1 for L=7.Therefore $P(X)=X^3 +X +1$ is primitive polynomial .

CLK	D1	D2	D3
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	1	0	1
6	0	1	0
7	0	0	1
8	1	0	0

Table1: Operation of 3-bit LFSR $P(X)=X^3 +X +1$

As an another example in fig.6. LFSR operation, consider a register that is 3-bits wide.
$P(x)= 1+X+X^2 + X^3$

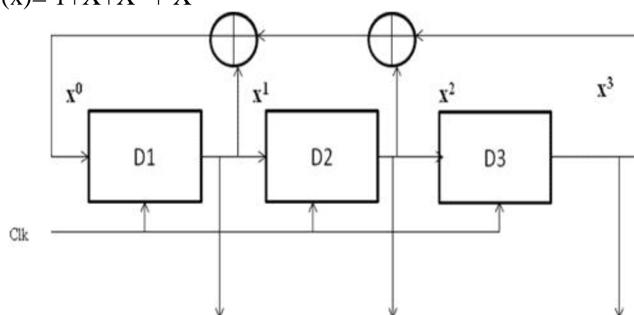

Fig 6. 3-bit LFSR Architecture(tap1,tap2)

Here n=3 $L= q^n -1$
For L=3; it result in remainder not equal to 1

For L=4; it result in remainder equal to 1

Therefore first condition is not satisfied i.e. remainder equal to 1 for L=4. Thus $P(x)= 1+X+X^2 + X^3$ is not a primitive polynomial then it not generates maximum-length sequence i.e. $2^N -1$.

CLK	D1	D2	D3
1	1	0	0
2	1	1	0
3	0	1	1
4	0	0	1
5	1	0	0

Table2: Operation of 3-bit LFSR $P(x)= 1+X+X^2 + X^3$

V. PROPOSED METHOD

A. Algorithm for Low Power LFSR (RS-LFSR)

LFSR is a shift register which consists of series of flip flops and is used to generate test patterns for BIST externally. The initial value of LFSR is called seed value. It poses a significant effect on energy consumption [6]. The output that influences the input is called tap. LFSR is represented by a polynomial known as characteristic polynomial, which is used to determine appropriate feedback taps. A common clock signal is applied to the flip flops which enable the propagation of bits from input to output of flip flops. The correlation between the bits can be achieved by adding more number of test vectors which reduces the switching activity so that the power consumption is reduced.

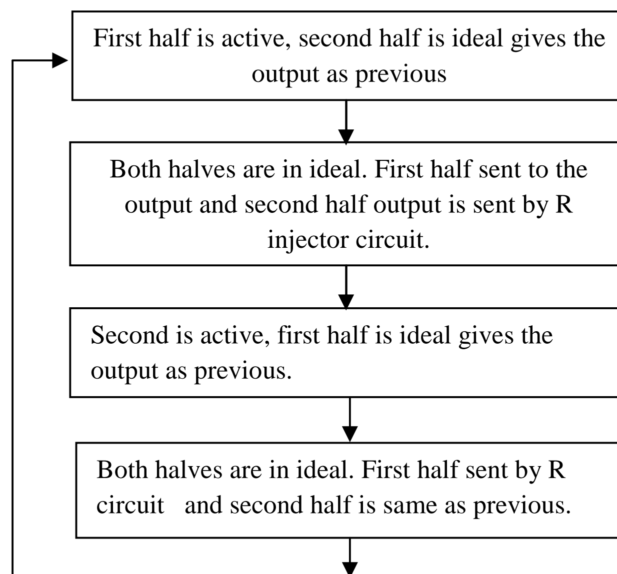

Fig. 7. Proposed LP LFSR

The TPG is activated by two non-overlapping enable signals (en1 and en2). Each enable signal activates one half of the LFSR. In other words, when en1en2=10, first half of the LFSR is active and the second half is in idle mode. The second half is active when en1en2=01. MUX selects either the injection bit or the exact bit in the LFSR.

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous; the generating test vector is T_i.

Step2: Both halves are idle First half sent to the output and second half's output is sent by the injection circuit, the generating test vector is T_{i1}.

Step3: Second half is active First half is in idle mode and gives out as previous; the generating test vector is T_{i2}.

Step4: Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is T_{i3}.

After completing step 4 again goes to step1 for generating test vector T_{i+1}.

The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip-flop to second level of hierarchy. Second

level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the RI injection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns.

VI. RESULTS

The Model Sim Mentor Graphics EDA tool is used in which conventional and Low Power LFSR is coded in verilog hardware description language. The outputs of Booth Multiplier and Array Multiplier Testing by using Low Power LFSR is Shown in Fig 8.1.and Low power LFSR .

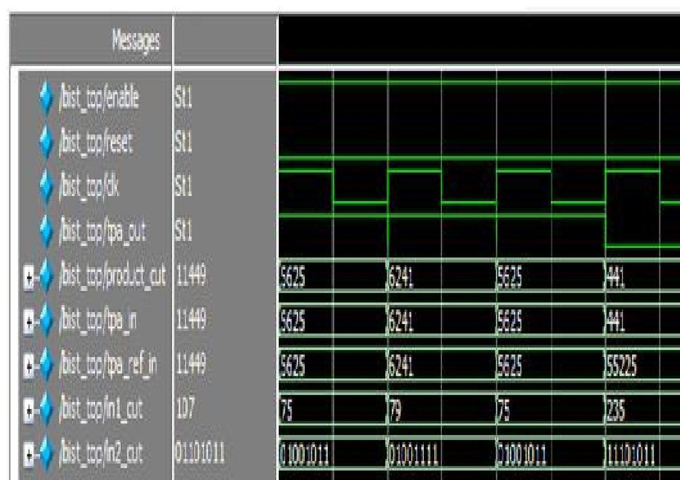

Fig. 8.1. Simulation Result of Booth Multiplier Testing Using LP- LFSR

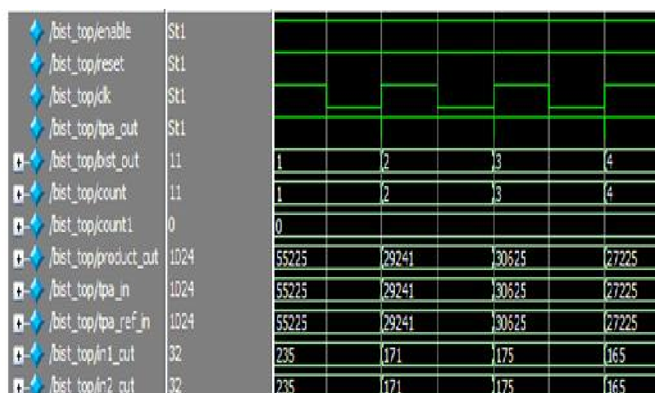

Fig. 8.2. Simulation Result of Array Multiplier Testing Using LP- LFSR

Module	Power(nw)
LFSR	7000.436
LP-LFSR	3010.595

Table3: Power LFSR and LP-LFSR

VII.CONCLUSION

For any of the circuit designed, there is need for testing of the circuit. For this purpose, random values are needed, and the random number generator is designed and it generates the random values. BIST is a design for testability (DFT) technique in which testing is carried out using built in hardware features. Since testing is built into the hardware, it is faster and efficient. The proposed test pattern generator reduces the switching activity among the test patterns which is more suitable for Built-In-Self-Test (BIST) structures used for testing of VLSI circuits. Circuits.

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