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Boost Interleaved Converter Integrated Voltage Multiplier Module for Renewable Energy System

[1]E Sandhya Rani, [2]Ch Vinod Kumar,[3]Y Srinivas Rao
[1]M.Tech Scholar,[2]Associate Professor,[3]Hod & Assistant Professor
Department of Electrical and Electronics Engineering, KIET-II Engineering College, Kakinada(AP), India
[1]ranisandhya605@gmail.com;[2]vinodkumar.ch15@gmail.com;[3]eenu.kiet@gmail.com

Abstract

This document presents a high step-up converter, which is apt for renewable energy system. Through a voltage multiplier unit composed of switched capacitors and coupled inductors, a conventional interleaved boost converter obtains high step-up gain without operating at extreme duty ratio. The design of the proposed converter not only reduces the current stress but also constrains the input current ripple, which decreases the conduction losses and lengthens the lifetime of the input source. In addition, due to the lossless passive clamp performance, leakage energy is recycled to the output terminal. Hence, large voltage spikes across the main switches are alleviated, and the efficiency is improved. Even the low voltage stress makes the low-voltage-rated MOSFETs be adopted for reductions of conduction losses and cost. Finally, the prototype circuit with 40-V input voltage, 380-V output, and 1000-W output power is operated to verify its performance. The highest efficiency is 97.1%.

Index Terms - Voltage multiplier module. Boost–flyback converter, high step-up, photovoltaic (PV) system.

I. Introduction

Currently renewable energy is progressively more valued and employed worldwide because of energy shortage and environmental contamination [1]–[7]. Renewable energy systems produce low voltage output, and thus, high step-up dc/dc converters have been widely employed in many renewable energy applications such fuel cells, wind power generation, and photovoltaic (PV) systems [17]–[20]. Such systems convert energy from renewable sources into electrical energy and convert low voltage into high voltage via a step-up converter, which can convert energy into electricity using a grid-by-grid inverter or dc micro grid. Fig. 1 shows a typical renewable energy system that consists of renewable energy sources, a step-up converter, and an inverter for ac application. The high step-up conversion may require two-stage converters with cascade structure for enough step-up gain, which decreases the efficiency and increases the cost. Thus, a high step-up converter is seen as an important stage in the system because such a system requires a sufficiently high step-up conversion with high efficiency.

Theoretically, conventional step-up converters, such as the boost converter and flyback converter, cannot attain a high step-up conversion with high efficiency because of the resistances of elements or leakage inductance; also, the voltage stresses are large. Thus, in recent years, many novel high step-up converters have been developed [10]–[20]. Despite these advances, high step-up single-switch converters are unsuitable to operate at heavy load given a large input current ripple, which increases conduction losses. The conventional interleaved boost converter is an excellent candidate for high-power applications and power factor correction. Unfortunately, the step-up gain is limited, and the voltage stresses on semiconductor components are equal to output voltage. Hence, based on the aforementioned considerations, modifying a conventional interleaved boost converter for high step-up and high-power application is a suitable approach. To integrate switched capacitors into an interleaved boost converter may make voltage gain reduplicate, but no service of coupled inductors causes the step-up voltage gain to be limited. Oppositely, to integrate only coupled inductors into an interleaved boost converter may make voltage gain higher and adjustable, but no employment of switched capacitors causes the step-up voltage gain to be ordinary. Thus, the synchronous employment of coupled inductors and switched capacitors is a better concept; moreover, high step-up gain, high efficiency, and low voltage stress are achieved even for high-power applications.

The proposed converter is a conventional interleaved boost converter integrated with a voltage multiplier module, and the voltage multiplier module is composed of switched capacitors and coupled inductors. The coupled inductors can be designed to extend step-up gain, and the switched capacitors offer extra voltage conversion ratio. In addition, when one of the switches turns off, the energy stored in the magnetizing inductor will transfer via three respective paths; thus, the current distribution not only decreases the conduction losses by lower effective current but also makes currents through some diodes decrease to zero before they turn off, which alleviate diode reverse recovery losses.

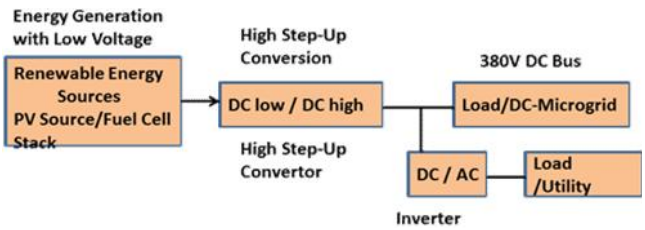


Fig. 1. Typical renewable energy system.

The advantages of the proposed converter are as follows.

1) The proposed converter is characterized by low input current ripple and low conduction losses, which increases the lifetime of renewable energy sources and makes it suitable for high-power applications.
2) The converter achieves the high step-up gain that renewable energy systems require.
3) Due to the lossless passive clamp performance, leakage energy is recycled to the output terminal. Hence, large voltage spikes across the main switches are alleviated, and the efficiency is improved.
4) Low cost and high efficiency are achieved by employment of the low-voltage-rated power switch with low *R*DS(ON); also, the voltage stresses on main switches and diodes are substantially lower than output voltage.
5) The inherent configuration of the proposed converter makes some diodes decrease conduction losses and alleviate diode reverse recovery losses.

II. Operating Principles

The proposed high step-up interleaved converter with a voltage multiplier module is shown in Fig. 2. The voltage multiplier module is composed of two coupled inductors and two switched capacitors and is inserted between a conventional interleaved boost converter to form a modified boost–flyback–forward interleaved structure. When the switches turn off by turn, the phase whose switch is in OFF state performs as a flyback converter, and the other phase whose switch is in ON state performs as a forward converter.

Primary windings of the coupled inductors with *Np* turns are employed to decrease input current ripple, and secondary windings of the coupled inductors with *Ns* turns are connected in series to extend voltage gain. The turn ratios of the coupled inductors are the same. The coupling references of the inductors are denoted by "·" and "∗".

The equivalent circuit of the proposed converter is shown in Fig. 3, where *Lm*1 and *Lm*2 are the magnetizing inductors; *Lk*1 and *Lk*2 represent the leakage inductors; *Ls* side; *S*1 and *S*2 denote the power switches; *Cc*1 and *Cc*2 are the switched capacitors; and *C*1, *C*2, and *C*3 are the output capacitors. *Dc*1 and *Dc*2 are the clamp diodes, *Db*1 and *Db*2 represent the output diodes for boost operation with switched capacitors, *Df*1 and *Df*2 represent the output diodes for flyback–forward operation, and *n* is defined as turn ratio *Ns/Np*.

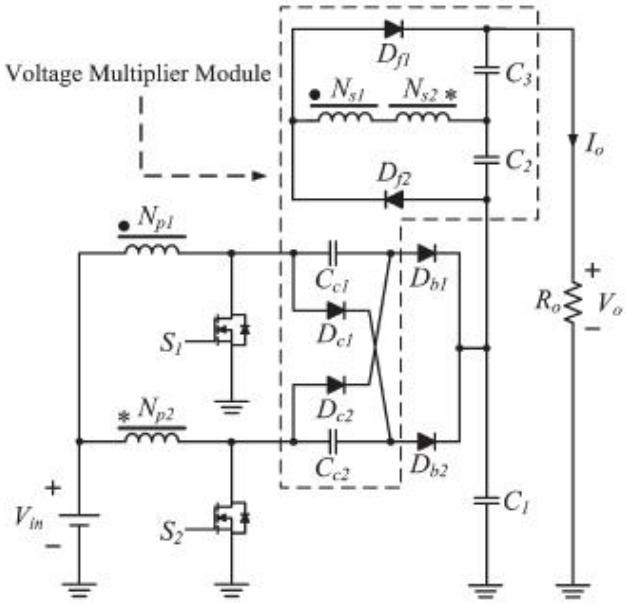


Figure.2. Proposed High Step-up converter

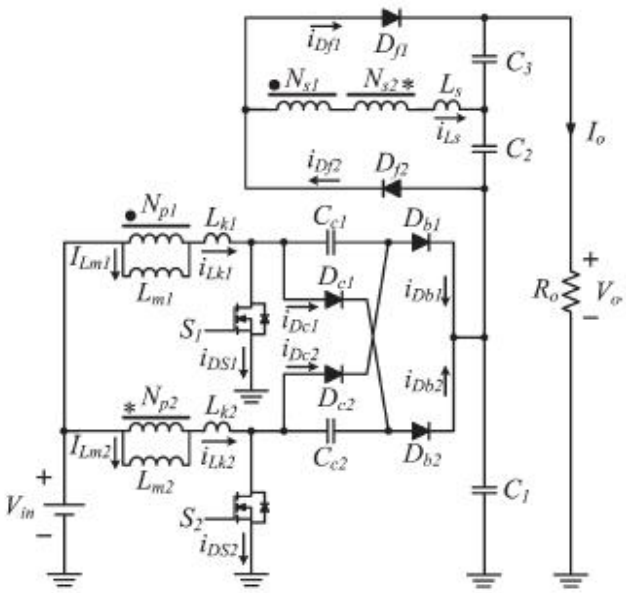


Figure.3. Equivalent circuit of the proposed converter

In the circuit analysis, the proposed converter operates in continuous conduction mode (CCM), and the duty cycles of the power switches during steady operation are greater than 0.5 and are interleaved with a 180◦ phase shift. The key steady waveform in one switching period of the proposed converter contains six modes, which are

depicted in Fig. 4, and Fig. 5 shows the topological stages of the circuit.

Mode I* [*t*0, *t*1]*: At $t = t0$, the power switch $S2$ remains in ON state, and the other power switch $S1$ begins to turn on. The diodes $Dc1$, $Dc2$, $Db1$, $Db2$, and $Df1$ are reversed biased, as shown in Fig. 5(a). The series leakage inductors Ls quickly release the stored energy to the output terminal via flyback–forward diode $Df2$, and the current through series leakage inductors Ls decreases to zero. Thus, the magnetizing inductor $Lm1$ still transfers energy to the secondary side of coupled inductors. The current through leakage inductor $Lk1$ increases linearly, and the other current through leakage inductor $Lk2$ decreases linearly.

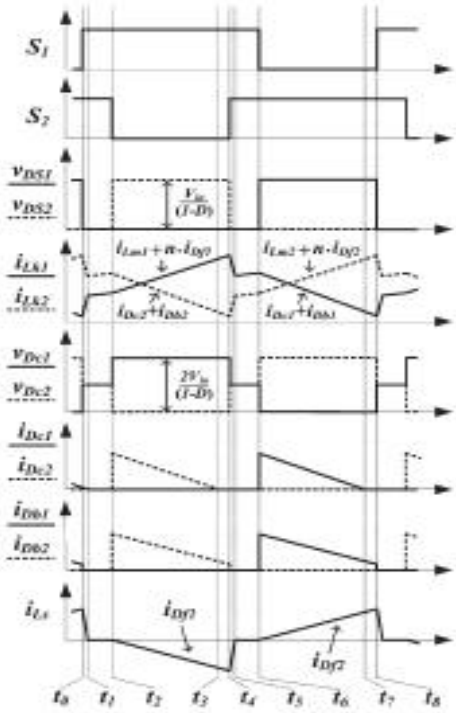


Fig. 4. Steady waveform of the proposed converter in CCM.

Mode II* [*t*1, *t*2]*: At $t = t1$, both of the power switches $S1$ and $S2$ remain in ON state, and all diodes are reversed biased, as shown in Fig. 5(b). Both currents through leakage inductors $Lk1$ and $Lk2$ are increased linearly due to charging by input voltage source Vin.

Mode III* [*t*2, *t*3]*: At $t = t2$, the power switch $S1$ remains in ON state, and the other power switch $S2$ begins to turn off. The diodes $Dc1$, $Db1$, and $Df2$ are reversed biased, as shown in Fig. 5(c). The energy stored in magnetizing inductor $Lm2$ transfers to the secondary side of coupled inductors, and the current through series leakage inductors Ls flows to output capacitor $C3$ via flyback–forward diode$Df1$. The voltage stress on power switch $S2$ is clamped by clamp capacitor $Cc1$ which equals the output voltage of the boost converter. The input voltage source, magnetizing inductor $Lm2$, leakage inductor $Lk2$, and clamp capacitor $Cc2$ release energy to the output terminal; thus, $VC1$ obtains a double output voltage of the boost converter.

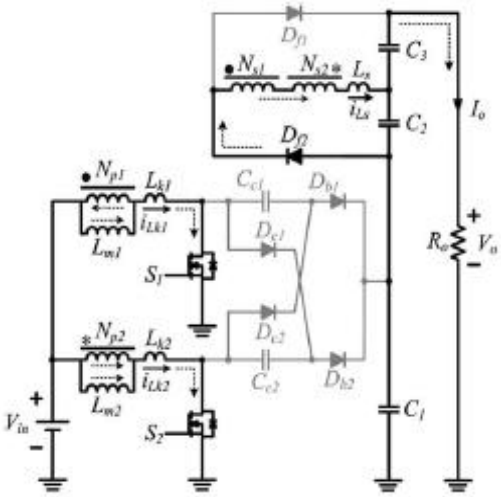
Mode IV* [*t*3, *t*4]*: At $t = t3$, the current $iDc2$ has naturally decreased to zero due to the magnetizing current distribution, and hence, diode reverse recovery losses are alleviated and conduction losses are decreased. Both power switches and all diodes remain in previous states except the clamp diode $Dc2$, as shown in Fig. 5(d).

Mode V* [*t*4, *t*5]*: At $t = t4$, the power switch $S1$ remains in ON state, and the other power switch $S2$ begins to turn on. The diodes $Dc1$, $Dc2$, $Db1$, $Db2$, and $Df2$ are reversed biased, as shown in Fig. 5(e). The series leakage inductors Ls quickly release the stored energy to the output terminal via flyback–forward diode $Df1$, and the current through series leakage inductors decreases to zero. Thus, the magnetizing inductor $Lm2$ still transfers energy to the secondary side of coupled inductors. The current through leakage inductor $Lk2$ increases linearly, and the other current through leakage inductor $Lk1$ decreases linearly.

Mode VI* [*t*5, *t*6]*: At $t = t5$, both of the power switches $S1$ and $S2$ remain in ON state, and all diodes are reversed biased, as shown in Fig. 5(f). Both currents through leakage inductors $Lk1$ and $Lk2$ are increased linearly due to charging by input voltage source Vin.

Mode VII* [*t*6, *t*7]*: At $t = t6$, the power switch $S2$ remains in ON state, and the other power switch $S1$ begins to turn off. The diodes $Dc2$, $Db2$, and $Df1$ are reversed biased, as shown in Fig. 5(g). The energy stored in magnetizing inductor $Lm1$ transfers to the secondary side of coupled inductors, and the current through series leakage inductors flows to output capacitor $C2$ via flyback–forward diode $Df2$. The voltage stress on power switch $S1$ is clamped by clamp capacitor $Cc2$ which equals the output voltage of the boost converter. The input voltage source, magnetizing inductor $Lm1$, leakage inductor $Lk1$, and clamp capacitor $Cc1$ release energy to the output terminal; thus, $VC1$ obtains double output voltage of the boost converter.

Mode VIII* [*t*7, *t*8]*: At $t = t7$, the current $iDc1$ has naturally decreased to zero due to the magnetizing current distribution, and hence, diode reverse recovery losses are alleviated and conduction losses are decreased. Both power switches and all diodes remain in previous states except the clamp diode $Dc1$, as shown in Fig. 5(h).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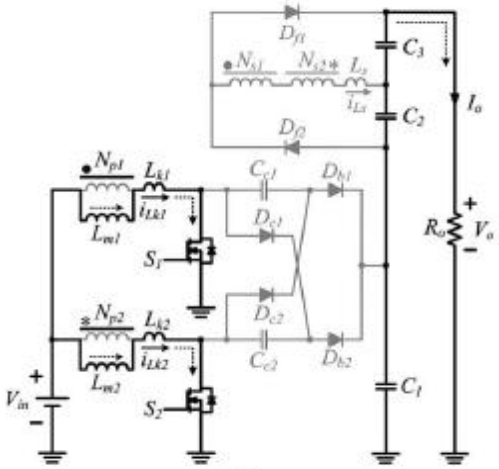
(a)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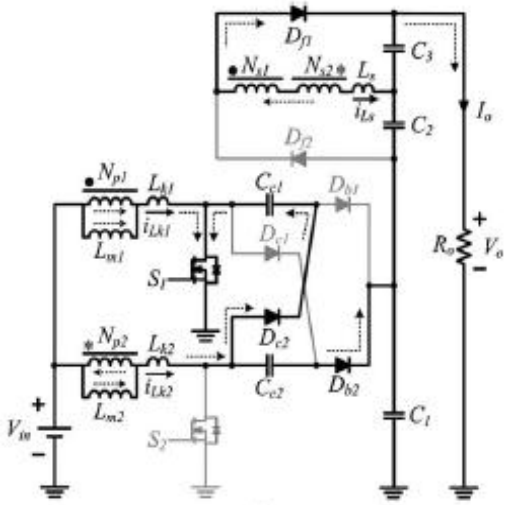
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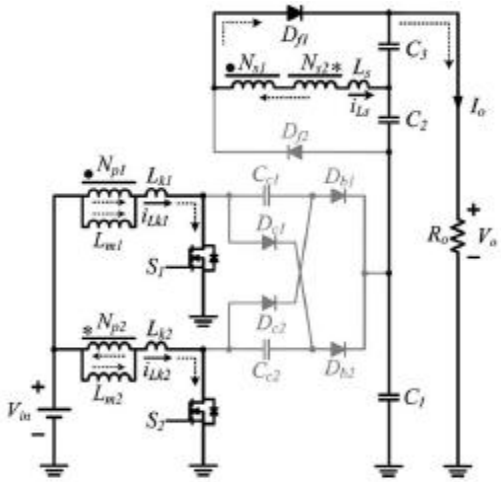
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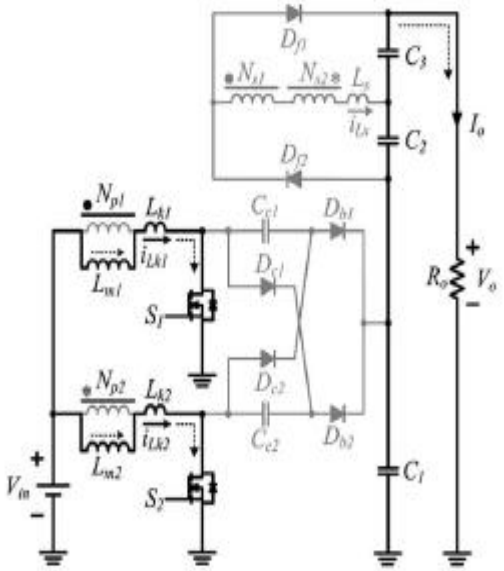
(e)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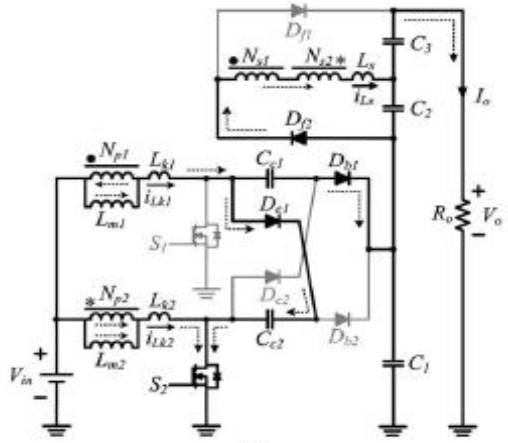
(f)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(g)

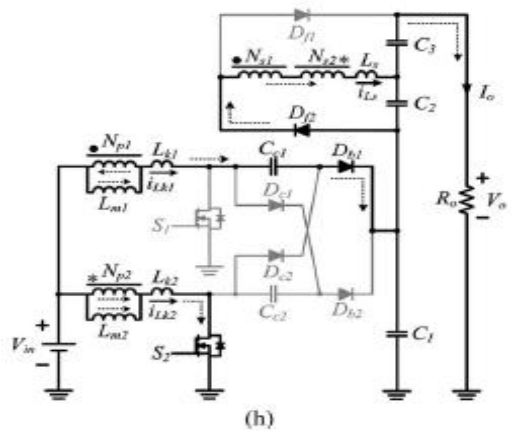


Fig.5. Operating modes of the proposed converter.
(a) Mode I [*to*, *t*1]. (b) Mode II [*t*1, *t*2].
(c) Mode III [*t*2, *t*3]. (d) Mode IV [*t*3, *t*4].
(e) Mode V [*t*4, *t*5]. (f) Mode VI [*t*5, *t*6].
(g) Mode VII [*t*6, *t*7]. (h) Mode VIII [*t*7, *t*8].

III. STEADY-STATE ANALYSIS

The transient characteristics of circuitry are disregarded to simplify the circuit performance analysis of the proposed converter in CCM, and some formulated assumptions are as follows.

1) All of the components in the proposed converter are ideal.
2) Leakage inductors *Lk*1, *Lk*2, and *Ls* are neglected.
3) Voltages on all capacitors are considered to be constant because of infinitely large capacitance.
4) Due to the completely symmetrical interleaved structure, the related components are defined as the corresponding symbols such as *Dc*1 and *Dc*2 defined as *Dc*.

A. Step-Up Gain

The voltage on clamp capacitor *Cc* can be regarded as an output voltage of the boost converter; thus, voltage *VCc* can be derived from

$$V_{Cc} = \frac{1}{1-D} V_{in} \quad (1)$$

When one of the switches turns off, voltage *VC*1 can obtain a double output voltage of the boost converter derived from

$$V_{C1} = \frac{1}{1-D} V_{in} + V_{Cc} = \frac{2}{1-D} V_{in} \quad (2)$$

The output filter capacitors *C*2 and *C*3 are charged by energy transformation from the primary side. When *S*2 is in ON state and *S*1 is in OFF state, *VC*2 is equal to the induced voltage of *Ns*1 plus the induced voltage of *Ns*2, and when *S*1 is in ON state and *S*2 is in OFF state, *VC*3 is also equal to the induced voltage of *Ns*1 plus the induced voltage of *Ns*2. Thus, voltages *VC*2 and *VC*3 can be derived from

$$V_{C2} = V_{C3} = n.V_{in}\left(1 + \frac{D}{1-D}\right) = \frac{n}{1-D} V_{in} \quad (3)$$

The output voltage can be derived from

$$V_0 = V_{C1} + V_{C2} + V_{C3} = \frac{2n+2}{1-D} V_{in} \quad (4)$$

In addition, the voltage gain of the proposed converter is

$$\frac{V_0}{V_{in}} = \frac{2n+2}{1-D} \quad (5)$$

Equation (5) confirms that the proposed converter has a high step-up voltage gain without an extreme duty cycle. The curve of the voltage gain related to turn ratio *n* and duty cycle is shown in Fig. 6. When the duty cycle is merely 0.6, the voltage gain reaches ten at a turn ratio *n* of one; the voltage gain reaches 30 at a turn ratio *n* of five.

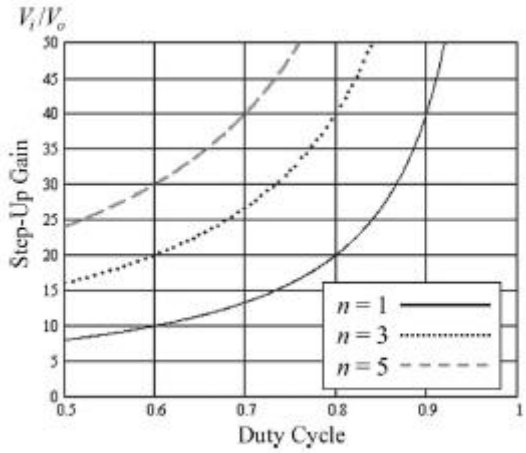


Fig. 6. Voltage gain versus turn ratio *n* and duty cycle.

B. Voltage Stress on Semiconductor Component

The voltage ripples on the capacitors are ignored to simplify the voltage stress analysis of the components of the proposed converter.

The voltage stress on power switch *S* is clamped and derived from

$$V_{S1} = V_{S2} = \frac{2}{1-D} V_{in} = \frac{1}{2n+2} V_o \quad (6)$$

Equation (6) confirms that low-voltage-rated MOSFET with low *R*DS(ON) can be adopted for the proposed converter to reduce conduction losses and costs. The voltage stress on the power switch *S* accounts for a fourth of output voltage *Vo*, even if turn ratio *n* is one. This feature makes the proposed converter suitable for high step-up and high-power applications.

The voltage stress on diode *Dc* is equal to *VC*1, and the voltage stress on diode *Db* is voltage *VC*1 minus voltage *VCc*. These voltage stresses can be derived from

$$V_{DC1} = V_{DC2} = \frac{2}{1-D}V_{in} = \frac{1}{n+1}V_o \qquad (7)$$

$$V_{Db1} = V_{Db2} = V_{C1} - V_{C2} = \frac{1}{1-D}V_{in} = \frac{1}{2n+2}V_o \qquad (8)$$

The voltage stress on diode *Db* is close to the voltage stress on power switch *S*. Although the voltage stress on diode *Dc* is larger, it accounts for only half of output voltage *Vo* at a turn ratio *n* of one. The voltage stresses on the diodes are lower as the voltage gain is extended by increasing turn ratio *n*. The voltage stress on diode *Df* equals the *VC*2 plus *VC*3, which can be derived from

$$V_{Df1} = V_{Df2} = \frac{2n}{1-D}V_{in} = \frac{n}{n+1}V_o \qquad (9)$$

Although the voltage stress on the diode *Df* increases as the turn ratio *n* increases, the voltage stress on the diodes *Df* is always lower than the output voltage.

The relationship between the voltage stresses on all the semiconductor components and the turn ratio *n* is illustrated in Fig. 7.

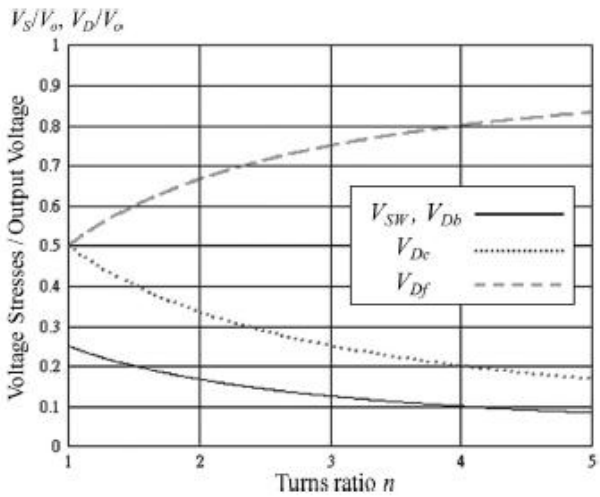


Fig. 7. Voltage stresses on semiconductor components versus turn ratio *n*.

C. Analysis of Conduction Losses

Some conduction losses are caused by resistances of semiconductor components and coupled inductors. Thus, all the components in the proposed converter are not assumed to be ideal, except for all the capacitors. Diode reverse recovery problems, core losses, switching losses, and the equivalent series resistance of capacitors are not discussed in this section. The characteristics of leakage inductors are disregarded because of energy recycling. The equivalent circuit, which includes the conduction losses of coupled inductors and semiconductor components, is shown in Fig. 8, in which *rL*1 and *rL*2 are the copper resistances of the primary windings of the coupled inductor; *rLs* represents the copper resistances of the secondary windings of the coupled inductors; *rDS*1 and *rDS*2 denote the on-resistances of power switches; *VDc*1, *VDc*2, *VDb*1, *VDb*2, *VDf*1, and *VDf*2 denote the forward biases of the diodes; and *rDc*1, *rDc*2, *rDb*1, *rDb*2, *rDf*1, and *rDf*2 are the resistances of the diodes.

Small-ripple approximation was used to calculate conduction losses. Thus, all currents that pass through components were approximated by the dc components. The magnetizing currents and capacitor voltages are assumed to be constant because of the infinite values of magnetizing inductors and capacitors. Finally, through voltage-second balance and capacitor-charge balance, the voltage conversion ratio with conduction losses can be derived from

$$\frac{Vo}{V_{in}} = \frac{\frac{2n+2}{1-D} - \frac{1}{V_{in}}.(V_{Dc} + V_{Db} + 2V_{Db} + 2V_{Df})}{1 + \frac{(2d-1)r_w + r_x}{R_o.(1-D)^2} + \frac{(2D-1)r_y + r_z}{R_o.(1-D)}} \qquad (10)$$

Where

$$r_w = [2(2-D)(n+1) - 1.5]r_{Ds} + 4n(1-D)r_{Dc}$$
$$r_x = [2n(2n+1)r_{Ds} + (2n+2)(2nD + 2D - 1)r_L]$$
$$r_y = [2(1-2n)r_{Dc} + 0.5r_{Db}]$$
$$r_w = [4n^2 r_L + 2(r_{Ls} + r_{Df}]$$

Because the turn ratio *n* and copper resistances of the secondary windings of the coupled inductors are directly proportional, the copper resistances of the coupled inductors can be expressed as

$$r_{Ls} = 2n.r_L$$

Efficiency is expressed as follows:

$$\eta = \frac{1 - \frac{1-D}{V_{in}(2n+2)}.(V_{Dc} + V_{Db} + 2V_{Df})}{1 + \frac{(2D-1).r_w + r_x}{R_o(1-D)^2} + \frac{(2D-1).r_y + r_z}{R_o(1-D)}} \qquad (11)$$

On the basis of (11), it can be inferred that the efficiency will be higher if the input voltage is considerably higher than the summation of the forward biases of all the diodes or if the resistance of the load is substantially larger

than the resistances of coupled inductors and semiconductor components. In addition, the maximal effect for efficiency is duty cycle, and the secondary is the copper resistance of coupled inductors.

D. Performance of Current Distribution

The inherent configuration of the proposed converter makes the energy stored in magnetizing inductors transfer via three respective paths as one of the switches turns off. Thus, the conduction losses by lower current distribution decreases the effective value of current and increases the capacity by lower peak value of current. In addition, if the load is not heavy enough, currents through some diodes decrease to zero before they turn off, which alleviate diode reverse recovery losses.

Under light-/medium-load condition, the currents through diodes *Db* and *Dc* decrease to zero before they turn off. When the load is continuously added, only the current *iDc* decreases to zero before diode *Dc* turns off. Under heavy load, although every current through the diode cannot decrease to zero before the related diode turns off, the reduction of conduction losses and the increase of capacity still perform well

E. Consideration for Applications of Renewable Energy Source and Low-Voltage Source

Many low-voltage sources, such as battery, and renewable energy sources, such as solar cell or fuel cell stack, need a high step-up conversion to supply power to high-voltage applications and loads. However, an excellent high step-up converter not only supplies efficient step-up conversion but also should lengthen the lifetime of sources such as battery set and fuel cell stack. Thus, suppression of input current ripple for lengthening the lifetime of sources is also a main design consideration.

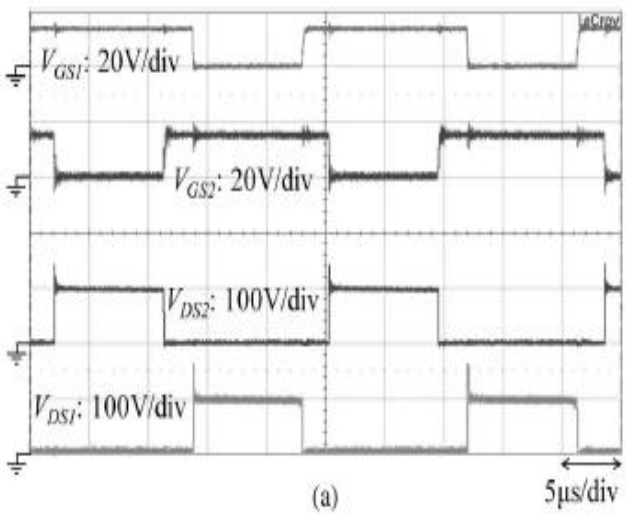
The proposed converter can satisfy the aforementioned applications even for high-power load due to the interleaved structure, which makes the power source or battery set discharge smoothly. The proposed converter operated in CCM is even more suitable than that operated in discontinuous conduction mode (DCM) for suppression of input current ripple, because the peak current in DCM is larger. For PV system, maximum power point tracking (MPPT) is an important consideration, and MPPT is implemented by adjusting the duty cycle within a range. However, the duty cycles of the proposed converter are greater than 0.5 due to the interleaved structure. Thus, if the proposed converter operates in some PV system, which must be satisfied with enough output voltage, duty cycle limitation, and MPPT, the turn ratio *n* should be set to make the maximum power point easily located in duty cycles greater than 0.5. The turn ratio *n* can be decreased slightly as a suitable value based on (5), which makes the duty cycle increase. Oppositely, a tradeoff should be made for practical output power to load between efficiency of the converter and MPPT, because the larger duty cycle causes efficiency to decrease even if copper resistances decreased by smaller turn ratio *n*.

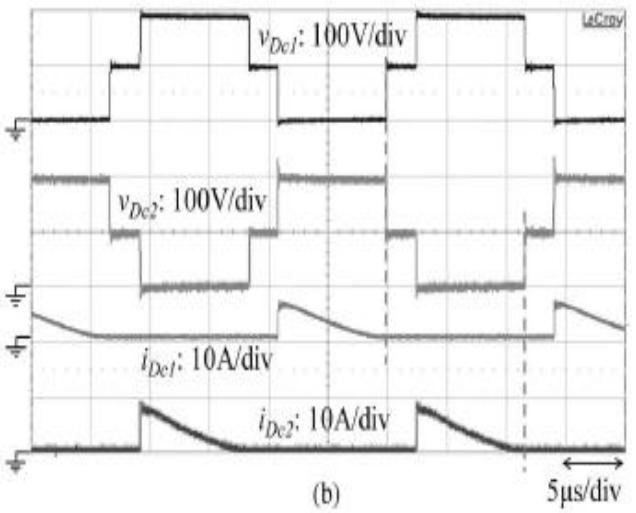
This section provides important information on characteristic analysis, feature, and consideration, which indicates the relationship among duty cycle, turn ratio, and components. The proposed converter for each application can be designed on the basis of selected turn ratios, components, and other considerations.

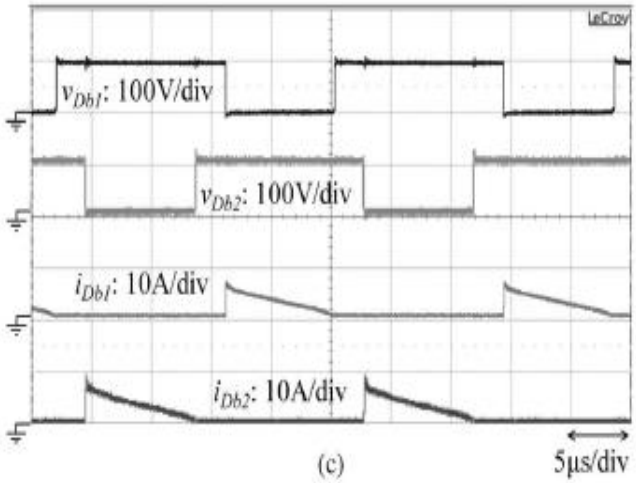
F. Performance Comparison

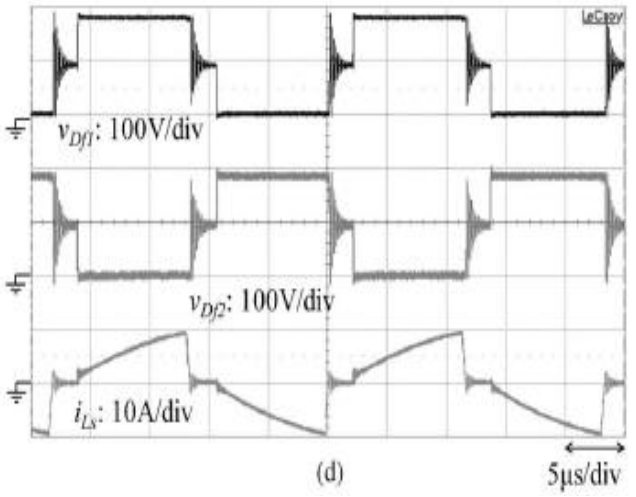
For demonstrating the performance of the proposed converter, the proposed converter and the other high step-up interleaved converters introduced in and are compared, as shown in Table I. The high step-up interleaved converter introduced in [36] is favorable for dc-microgrid applications, and the other high step-up interleaved converter introduced in [40] is suitable as a candidate for high step-up high-power conversion of the PV system. Both of the converters use coupled inductors and switched capacitors to achieve high step-up conversion.

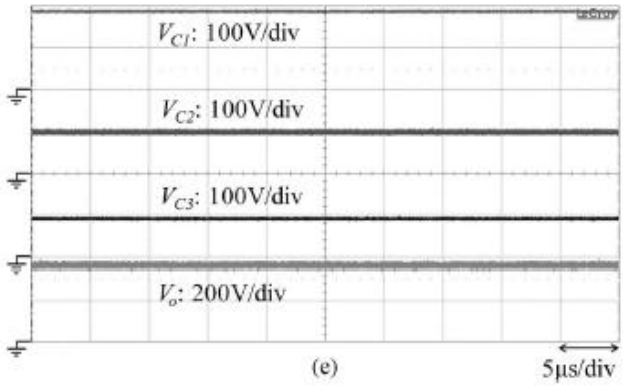
The step-up gain of the proposed converter is the highest, and the voltage stresses on semiconductor devices are the lowest. In addition, the extra winding or core may result in the circuit being costly and bulky. The proposed converter only uses two normal coupled inductors; thus, the cost and degree of difficulty of design are lower. Oppositely, the performances of current sharing and distribution make the reliability, capacity, and efficiency higher. Thus, the proposed converter is suitable for high step-up high-power applications.











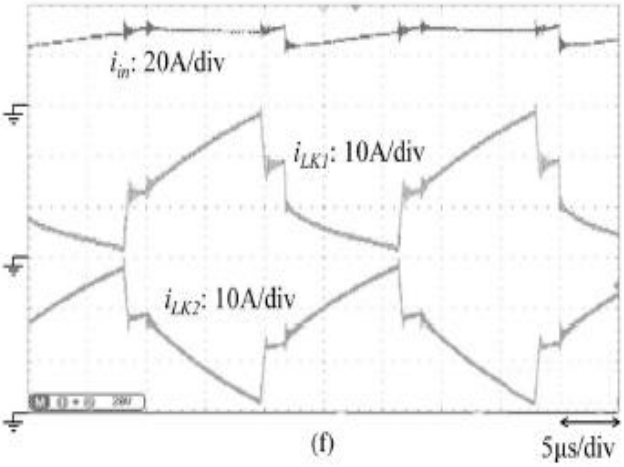


Fig. 9. Measured waveforms at full load of 1000 W.

IV. Design And Experiment Of Proposed Converter

A 1-kW prototype of the proposed high step-up converter is tested. The electrical specifications are *V*in = 40 V, *Vo* = 380 V, and *fs* = 40 kHz. The major components have been chosen as follows: Magnetizing inductors *Lm*1 and *Lm*2 = 133 *μ*H; turn ratio *n* = 1; power switches *S*1 and *S*2 are IRFP4227; diodes *Dc*1 and *Dc*2 are BYQ28E-200; diodes *Db*1, *Db*2, *Df*1, and *Df*2 are FCF06A-40; capacitors *Cc*1, *Cc*2, *C*2, and *C*3 = 220 *μ*F; and *C*1 = 470 *μ*F.

The design consideration of the proposed converter includes component selection and coupled inductor design, which are based on the analysis presented in the previous section. In the proposed converter, the values of the primary leakage inductors of the coupled inductors are set as close as possible for current sharing performance, and the leakage inductors *Lk*1 and *Lk*2 are 1.6 *μ*H. Due to the performances of high step-up gain, the turn ratio *n* can be set as one for the prototype circuit with 40-V input voltage and 380-V output to reduce cost, volume, and conduction loss of the winding. Thus, the copper resistances which affect efficiency much can be decreased.

Fig. 9 shows the measured waveforms at full load of 1000W. Fig. 9(a) shows the interleaved pulsewidth-modulation signals *Vgs*1 and *Vgs*2, as well as the voltage stresses on the power switches. *VDS*1 and *VDS*2 are

clamped at 100 V, which is much lower than the output voltage. Fig. 9(b) shows the voltage stresses on clamp diodes and the current through clamp diodes. The voltage stresses *vDc*1 and *vDc*2 are doubles of *VDS*1 and *VDS*2. The currents *iDc*1 and *iDc*2 decrease to zero before they turn off, which alleviate diode reverse recovery losses. Fig. 9(c) shows the waveform of *vDb*1, *vDb*2, *iDb*1, and *iDb*2.

The voltage stresses *vDb*1 and *vDb*2 are equal to the voltage stresses on power switches. Fig. 9(d) shows the waveform of *vDf*1, *vDf*2, and *iLs*. The voltage stresses *vDf*1 and *vDf*2 are equal to *vDc*1 and *vDc*2 because the turn ratio *n* is set as one, and the ringing characteristics are caused by the series leakage inductors *Ls*. Fig. 9(e) shows the output voltage and voltages on output capacitors. The output voltage *Vo* is 380 V. Because the turn ratio *n* is set as one, the voltages *VC*2 and *VC*3 are half of *VC*1. From experimental results, it can be proved that the voltages on output capacitors are in accordance with those of steady-state analysis, and all of the measured voltage stresses are corresponding to those in Fig. 7, which are illustrated by theoretical analysis. Fig. 9(f) shows the input current *I*in and each current through the primary leakage inductor, which demonstrates the performance of current sharing.

Fig. 10 shows the measured efficiency of the proposed converter. The maximum efficiency is 97.1% at *Po* = 400 W. At full load of 1 kW, the conversion efficiency is about 96.4%.

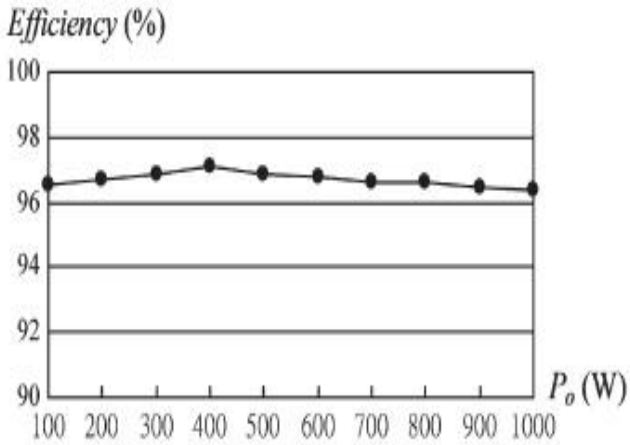


Fig. 10. Measured efficiency of the proposed converter.

V. Conclusion

This document has presented the theoretical analysis of steady state, related consideration, simulation results, and experimental results for the proposed converter. The proposed converter has successfully implemented an efficient high step-up conversion through the voltage multiplier module. The interleaved structure reduces the input current ripple and distributes the current through each component. In addition, the lossless passive clamp function recycles the leakage energy and constrains a large voltage spike across the power switch. Meanwhile, the voltage stress on the power switch is restricted and much lower than the output voltage (380 V). Furthermore, the full-load efficiency is 96.4% at *Po* = 1000 W, and the highest efficiency is 97.1% at *Po* = 400 W. Thus, the proposed converter is suitable for high-power or renewable energy applications that need high step-up conversion.

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Author :

E.Sandhya Rani received B.Tech degree from Kakinada Institute of Engineering & Technology for Women in 2012. Presently she is pursuing M.Tech in the Department of Electrical and Electronics Engineering in Kakinada Institute Of Engineering and Technology-II from JNTUK. Her areas of interest are Power Electronics and Drives.

Ch. Vinod Kumar received his B.Tech. degree from Jawaharlal Nehru Technological University, India, in 2005 and the M.Tech. degree from Jawaharlal Nehru Technological University-Kakinada, in 2009, both in electrical engineering, Since 2005, he has been an Assistant Professor till 2007 and HOD & Associate Professor from 2010 in the Department of Electrical and Electronics Engineering, KIET -II Engineering College. Currently working as Associate Professor in KIET -II Engineering College. His current research interests include motor drives, design and control of power electronic converters / systems, inverter-based distributed generation, hybrid electric vehicle, power systems.

Y.Srinivasa Rao completed his BTech in the Department of Electrical and Electronics Engineering in Kakinada Institute Of Engineering and Technology in 2008 and MTech in 2012. He worked as Assistant Professor in the Department of Electrical and Electronics Engineering in Kakinada Institute Of Engineering and Technology from 2010 to 2014. Now working as HOD & Assistant Professor in KIET-II Engineering College. His area of interest is Power Systems.