



A high Step-up DC-DC Converter employs Cascading Cockcroft-Walton Voltage Multiplier by omitting Step-up Transformer

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Abstract: In my paper possess a high voltage gain and devoid of using Step up transformer through a high step-up DC-DC converter based on Cockcroft-Walton (CW) voltage multiplier. Here the input was in low to DC voltage is boost up with the help of boost inductor in DC-DC converter. The n-number of stages CW-voltage multiplier is applying input as low to AC voltage to high output DC voltage. This afford gets a continuous input current with low ripple, high voltage gain, reduced switching losses, low voltage stress on the switches, diodes & capacitors and also improving efficiency of the converter. In my paper, strategic controlled steps retain two independent frequencies, one of which operates at high frequency to optimized size of the inductor while the other one operates at comparatively low in frequency according to the desired output voltage ripple. Finally this converter is authorized by simulation and experimental result is designed.

Key words: CW-Cockcroft-Walton, Boost inductor, Output voltage ripple.

I. Introduction

The conventional boost DC-DC converter can provide a very high voltage gain by using an extreme high duty cycle. The step-up dc-dc converters have been proposed to obtain high voltage ratios without extreme high duty cycle by using isolated transformers or coupled inductors. Among these high step-up dc-dc converters, voltage-fed type sustains high input current ripple. Thus, providing low input current ripple and high voltage ratio, current-fed converters are generally superior to their counterparts. However, in order to achieve high voltage gain, the leakage inductance of the

transformer is relatively increased due to the high number of winding turns. Consequently, the switch is burdened with high voltage spikes across the switch at the turn-off instant. Thus, higher voltage-rating switches are required. The current fed converters are providing low input current ripple and high voltage ratio. Modified current-fed converters integrated with step-up transformers or coupled-inductors which focused on improving efficiency and reducing voltage stress, were presented to achieve high voltage gain without extreme high duty cycle.

The design of high-frequency transformers, coupled inductors or resonant components for these converters are relatively complex compared with the conventional boost DC-DC converter. The step-up DC-DC converters without step-up transformers and coupled inductors were presented. By cascading diode-capacitor or diode-inductor modules, these kinds of DC-DC converters provide not only high voltage gain but also simple and robust structures.

The conventional Cockcroft-Walton voltage multiplier is very popular among high voltage DC applications. Replacing the step-up transformer with the boost type structure, the proposed converter provides higher voltage ratio than that of the conventional CW voltage multiplier.

II. Steady state Analysis

The proposed converter is supplied by a low-level dc source, such as battery, PV module or fuel cell sources. The proposed converter consists of one boost inductor L_s , four switches (S_{m1} , S_{m2} , S_{c1} , and S_{c2}), and one n -stage CW voltage multiplier. S_{m1} (S_{c1}) and S_{m2} (S_{c2}) operate in complementary mode, and the

operating frequencies of S_{m1} and S_{c1} are defined as f_{sm} and f_{sc} , respectively. For convenience, f_{sm} is denoted as modulation frequency and f_{sc} is denoted as alternating frequency. Theoretically, these two frequencies should be as high as possible, so that smaller inductor and capacitors can be used in this circuit. In this paper, f_{sm} is set much higher than f_{sc} , and the output voltage is regulated by controlling the duty cycle of S_{m1} and S_{m2} , while the output voltage ripple can be adjusted by f_{sc} . As shown in Fig.1, the well-known CW voltage multiplier is constructed by a cascade of stages with each stage containing two capacitors and two diodes. In an n -stage CW voltage multiplier, there are $N (=2n)$ capacitors and N diodes.

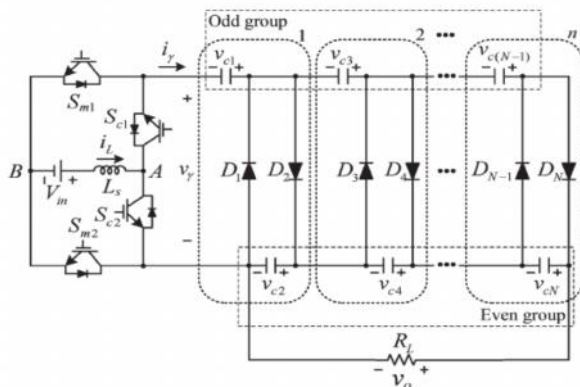


Fig.1 Proposed converter with n -stage CW voltage multiplier

III. Mathematical Model

As shown in Fig.1 the proposed converter is an integration of a boost converter with a CW voltage multiplier. For analysis, the equivalent circuit of the proposed converter can be divided into source-side and load-side parts. For the source-side part, the conducting states d_{sc} and d_{sm} are defined in Table I, where strategy I does not include safe commutation and strategy II includes safe commutation. According to the conducting states d_{sc} and d_{sm} , the differential equation of the inductor current is given by

$$\frac{di_L}{dt} = \frac{1}{L_s} [V_{in} - (d_{sc} - d_{sm}) \cdot v_\gamma] \quad (1)$$

TABLE I
CONDUCTING STATES OF FOUR SWITCHES

Conducting states		Strategy I	Strategy II
d_{sc}	d_{sm}	$S_{c1}, S_{c2}, S_{m1}, S_{m2}$	
0	0	0101	0111
0	1	0110	0110
1	1	1010	1011
1	0	1001	1001
1	1		
or	or	-	1111
0	0		

where V_{in} is the input voltage, i_L is the input current, and v_γ is the terminal voltage of the CW voltage multiplier. Assuming that the converter operates in CCM, the current i flowing into the CW voltage multiplier depends on d_{sm} and d_{sc} and can be expressed as

$$i_\gamma = (d_{sc} - d_{sm}) \cdot i_L \quad (2)$$

where the current i can be deemed a pulse-form current source. In, the mathematical model of an n -stage CW voltage multiplier was discussed and simplified the equivalent circuit, which was convenient for simulation work.

Circuit operation principle

In order to simplify the analysis of circuit operation, the proposed converter with a three-stage CW voltage multiplier, as shown in Fig3.1. is used Before analyzing, some assumptions are made as follows.

- 1) All of the circuit elements are ideal, and there is no power loss in the system.
- 2) 2) When a high-frequency periodic alternating current is fed into the CW circuit and all of the capacitors in the CW voltage multiplier are sufficiently large, the voltage drop and ripple of each capacitor voltage can be ignored under a

reasonable load condition. Thus, the voltages across

- 3) all capacitors are equal, except the first capacitor whose voltage is one half of the others.
- 4) 3) The proposed converter is operating in CCM and in the steady-state condition.
- 5) 4) When the inductor transfers the storage energy to the CW circuit, only one of the diodes in the CW circuit will be conducted.
- 6) 5) Some safe commutation states are ignored.

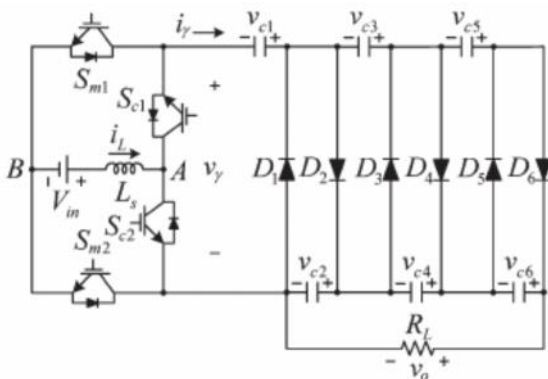


Fig.3.1 Converter with three-stage CW voltage multiplier

According to the second assumption, each capacitor voltage in the CW voltage multiplier can be defined as

$$v_{ck} = \begin{cases} V_c/2 & \text{for } k = 1 \\ V_c & \text{for } k = 2, 3, \dots, N \end{cases} \quad (1)$$

where v_{ck} is the voltage of the k th capacitor and V_c is the steady-state voltage of $v_{c2}-v_{cN}$. For an n -stage CW voltage multiplier, the output voltage is equal to the total voltage of

all even capacitors, which can be expressed as

$$V_o = nV_c. \quad (16)$$

Substituting (16) into (15), each capacitor voltage in an n -stage CW voltage multiplier can also be expressed as

$$v_{ck} = \begin{cases} V_o/2n & \text{for } k = 1 \\ V_o/n & \text{for } k = 2, 3, \dots, N \end{cases} \quad (17)$$

where V_o is the steady-state voltage of the output load side.

Fig.3.2 shows the theoretical waveforms of the proposed converter, including switching signals, inductor current, v , i , and diode currents. According to the polarity of i , the operation of the proposed converter can be divided into two parts: positive conducting interval $[t_0, t_1]$ for $i \geq 0$ and negative conducting interval $[t_1, t_2]$ for $i \leq 0$. During positive conducting interval, only one of the even diodes can conduct with the sequence $D_6-D_4-D_2$, while during negative conducting interval, only one of the odd diodes can conduct with the sequence $D_5-D_3-D_1$. Moreover, during positive conducting interval, there are four circuit states, as shown in Fig.3.3(a)-(d), denoted as states I, II-A, II-B, and II-C. In state I, S_{m1} turns on; thus, the energy stored in the inductor increases. In states II-A, II-B, and II-C, S_{m2} turns on, and the inductor transfers energy to the CW circuit through D_6 , D_4 , and D_2 , respectively. Similarly, there are four circuit states in the negative conducting interval, as shown in Fig.3.3(e)-(h), denoted as

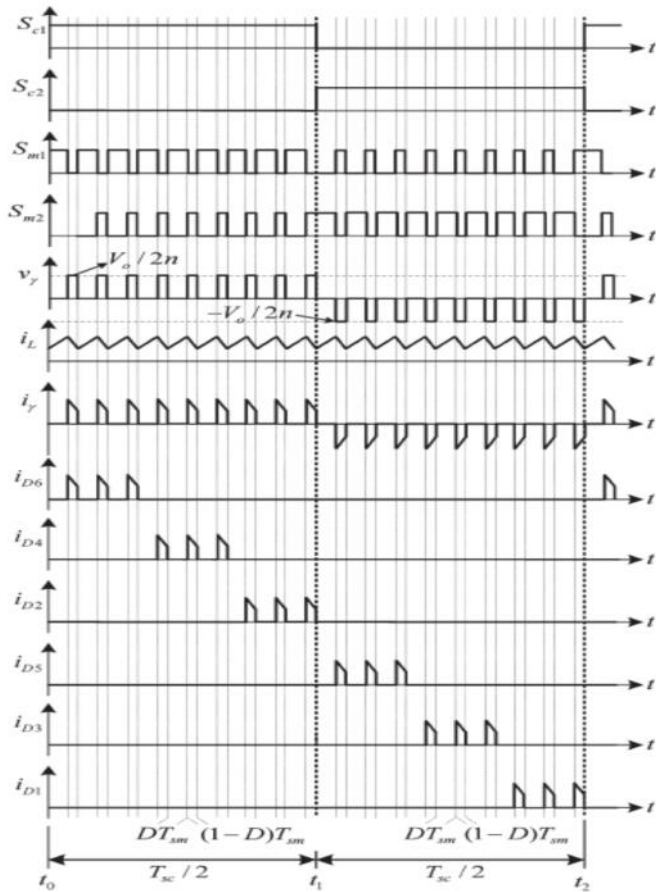


Fig.3.2 Ideal waveforms of the proposed converter in CCM.

states III, IV-A, IV-B, and IV-C. According to Fig. 3.3, the circuit operation principle of the proposed converter is illustrated in detail as follows.

1) State I: $Sm1$ and $Sc1$ are turned on, and $Sm2$, $Sc2$, and all CW diodes are turned off, as shown in Fig.3.3(a). The boost inductor is charged by the input dc source, the even-group capacitors $C6$, $C4$, and $C2$ supply the load, and the odd-group capacitors $C5$, $C3$, and $C1$ are floating.

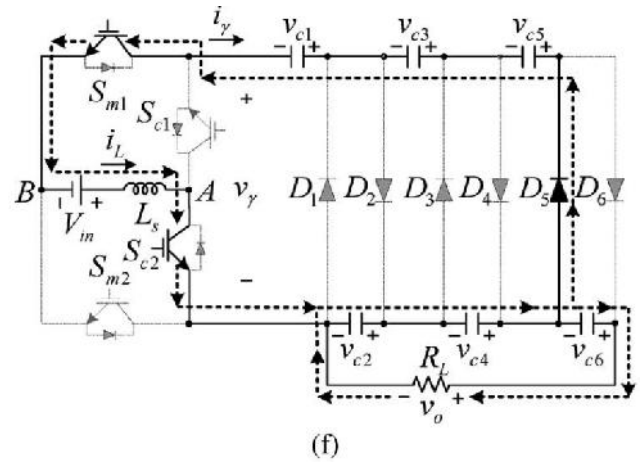
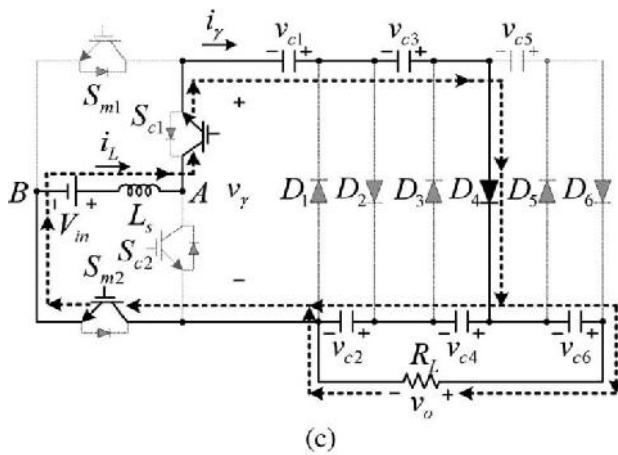
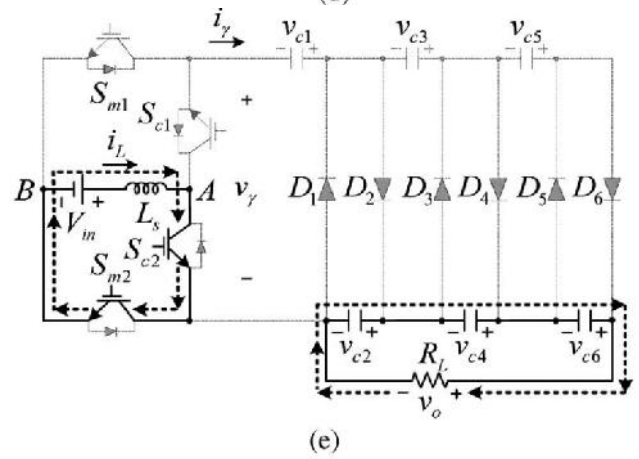
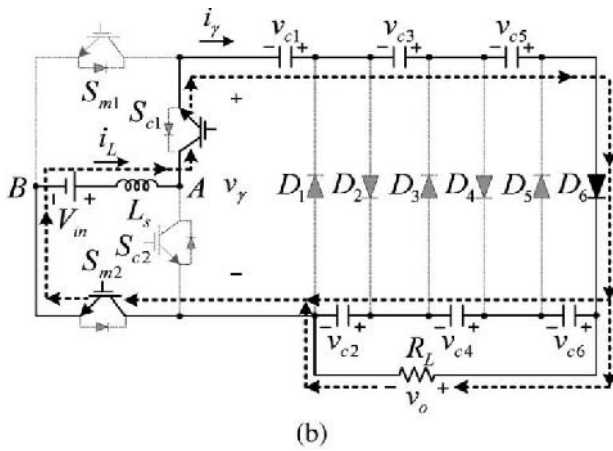
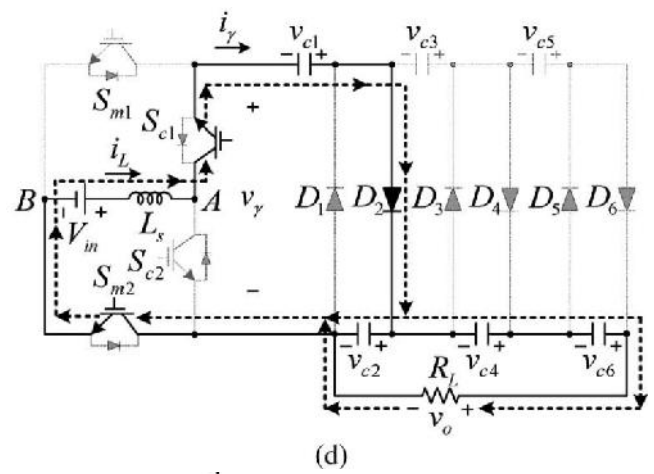
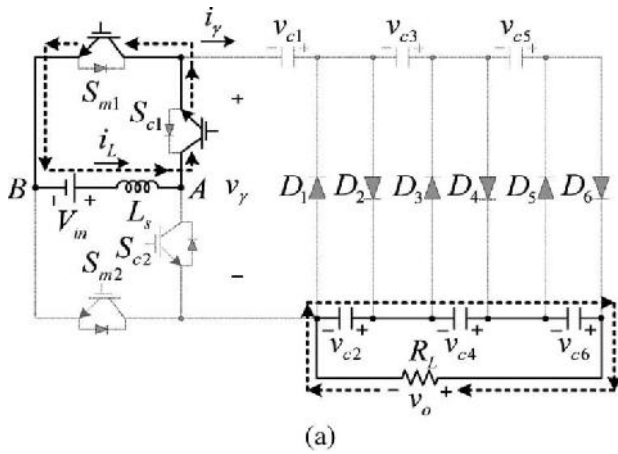
2) State II: $Sm2$ and $Sc1$ are turned on, $Sm1$ and $Sc2$ are turned off, and the current i is positive. The boost inductor and input dc

source transfer energy to the CW voltage multiplier through different even diodes, as shown in Fig.3.3 (b)–(d). In Fig.3.3(b), state II-A, $D6$ is conducting; thus, the even-group capacitors $C6$, $C4$, and $C2$ are charged, and the odd-group capacitors $C5$, $C3$, and $C1$ are discharged by i . In Fig.3.3 (c), state II-B, $D4$ is conducting. Thus, $C4$ and $C2$ are charged, $C3$ and $C1$ are discharged by i , $C6$ supplies load current, and $C5$ is floating. In Fig.3.3 (d), state II-C, $D2$ is conducting. Thus, $C2$ is charged, $C1$ is discharged by i , $C6$ and $C4$ supply load current, and $C5$ and $C3$ are floating.

3) State III: $Sm2$ and $Sc2$ are turned on, and $Sm1$, $Sc1$, and all CW diodes are turned off, as shown in Fig.3.3(e). The boost inductor is charged by the input dc source, the even group capacitors $C6$, $C4$, and $C2$ supply the load, and the odd-group capacitors $C5$, $C3$, and $C1$ are floating.

4) State IV: $Sm1$ and $Sc2$ are turned on, $Sm2$ and $Sc1$ are turned off, and the current i is negative. The boost inductor and input dc source transfer energy to the CW voltage multiplier through different odd diodes, as shown in Fig.3.3 (f)–(h). In Fig. 3.3 (f), state IV-A, $D5$ is conducting.

Thus, the even-group capacitors, except $C6$ which supplies load current, are discharged, and the odd-group capacitors $C5$, $C3$, and $C1$ are charged by i . In Fig.3.3(g), state IV-B, $D3$ is conducting. Thus, $C2$ is discharged, $C3$ and $C1$ are charged by i , $C6$ and $C4$ supply load current, and $C5$ is floating. In Fig.3.3 (h), state IV-C, $D1$ is conducting. Thus, $C1$ is charged by i , all even capacitors supply load current, and $C5$ and $C3$ are floating.



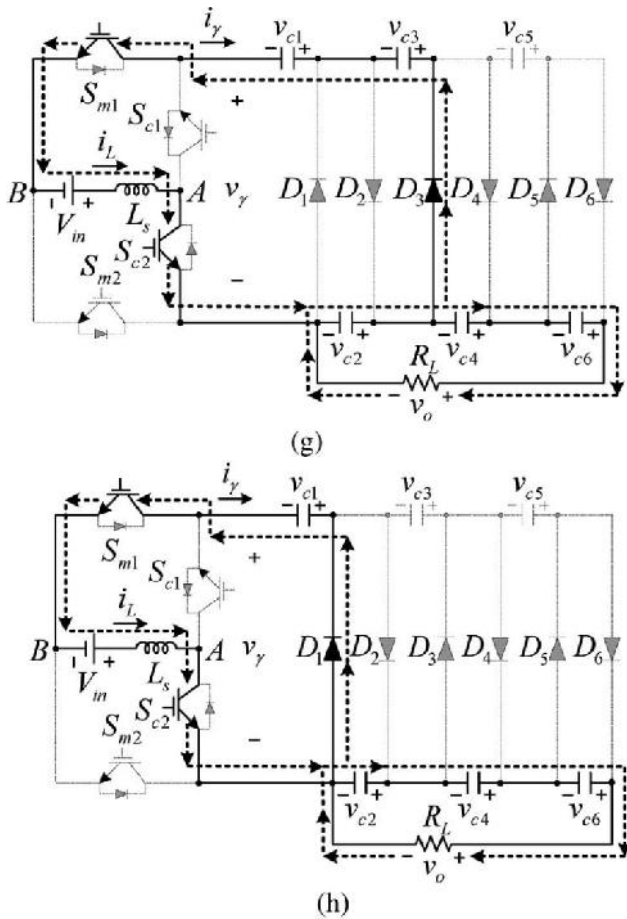


Fig.3.3 Conducting paths of proposed converter. (a) State I. (b) State II-A. (c) State II-B. (d) State II-C. (e) State III. (f) State IV-A. (g) State IV-B. (h) State IV-C

Design Considerations Of Proposed Converter:

In this, the voltage and current stresses on each capacitor, switch, and diode will be considered. Moreover, the values of inductor and capacitors Fig.4 (a-h) discussed as well.

Design Considerations:

- i. Capacitor Voltage Stress
- ii. Switch Voltage and Current Stresses
- iii. Diode Voltage and Current Stresses
- iv. Input Inductance
- v. Capacitance of CW Voltage Multiplier
- vi. Number of Major Components

Moreover, it can be seen that the difference of the number of major components between the proposed converter and the other converters increases when a higher voltage gain is desired.

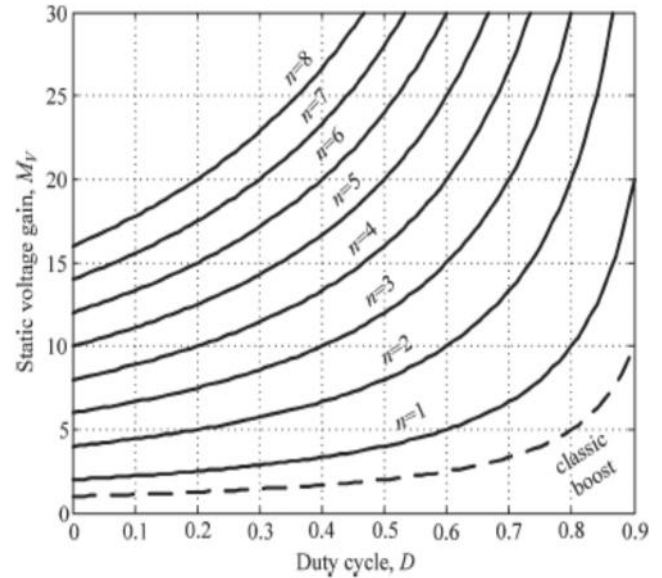


Fig. 5 Voltage gain versus duty cycle for the proposed converter under $n = 1-8$ and the classic boost dc-dc converter

TABLE II

Comparison of proposed converter and other converters

	Proposed converter	Converter shown in Fig. 1(a)	Converter shown in Fig. 1(b)	Converter shown in Fig. 1(c)
Voltage gain	$M_y = \frac{2n}{1-D}$	$M_y = \left(\frac{1}{1-D}\right)^n$	$M_y = \frac{n+D}{1-D}, n = \text{odd}$ $M_y = \frac{n+1-D}{1-D}, n = \text{even}$	$M_y = \frac{n+1}{1-D}$
Capacitor voltage	$V_{Ck} = \begin{cases} \frac{V_m}{1-D} & \text{for } k=1 \\ \frac{2V_m}{1-D} & \text{for } k=2, \dots, 2n \end{cases}$	$V_{Ck} = V_m \left(\frac{1}{1-D}\right)^k \text{ for } k=1, \dots, n$	$V_{Ck1} = V_{Ck2} = \frac{kV_m}{1-D} \text{ for } k=1, \dots, n$	$V_{Ck1} = \frac{kV_m}{1-D} \text{ for } k=1, \dots, n$ $V_{Ck2} = \frac{V_m}{1-D}$
Elements number	$N_{total} = 5+4n$	$N_{total} = 4n$	$N_{total} = 4+4n$	$N_{total} = 4+4n$
Switch voltage	$\frac{V_m}{1-D}$	$V_m \left(\frac{1}{1-D}\right)^n$	$\frac{V_m}{1-D}$	$\frac{V_m}{1-D}$
Diode voltage	$\frac{2V_m}{1-D}$	$\begin{cases} V_{Dk1} = V_{Ck} & \text{for } k=1, \dots, n \\ V_{Dk2} = V_{Ck} - V_{Ck} & \text{for } k=1, \dots, n-1 \end{cases}$	$\frac{V_m}{1-D}$	$\frac{V_m}{1-D}$

Control Strategy Of Proposed Converter:

Due to the circuit operation, the proposed converter is similar to the conventional boost dc-dc converter, except that the proposed converter provides alternating current i to the CW voltage multiplier. Thus, some commercial control ICs for conventional boost converters can adopt to the proposed converter with an extra auxiliary circuit which modifies the original PWM signal to signals with suitable timing and frequency for the four switches. Taking a close look at the circuit states in Fig. it can be found that $Sc1$ and $Sc2$ ($Sm1$ and $Sm2$) swap the conduction states at the changing instant between each state. If the commutation fails, the

discontinuous inductor current will cause voltage spike and damage the switching elements. However, the switching strategy, on the four switches of the proposed converter is not including safe commutation technique. Therefore, another switching strategy including safe commutation technique under the same output function is used in the control strategy of the proposed converter to avoid open circuit of the inductor.

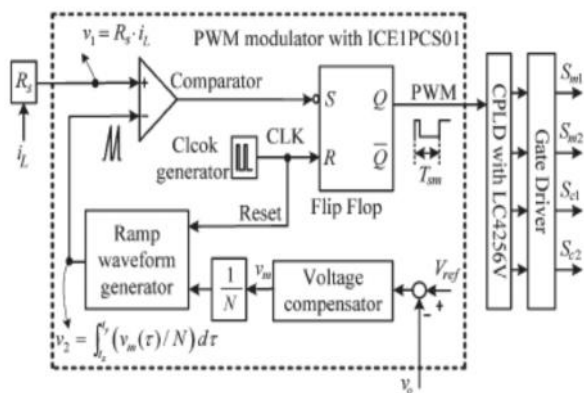


Fig. 6 Control strategy of proposed converter including safe commutation technique.

IV. Simulation Results

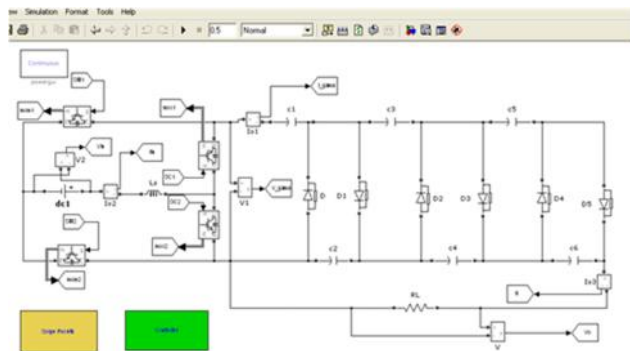


Fig. 7 High Step-up DC-DC Converter using Cascaded Cockcroft-Walton Voltage Multiplier

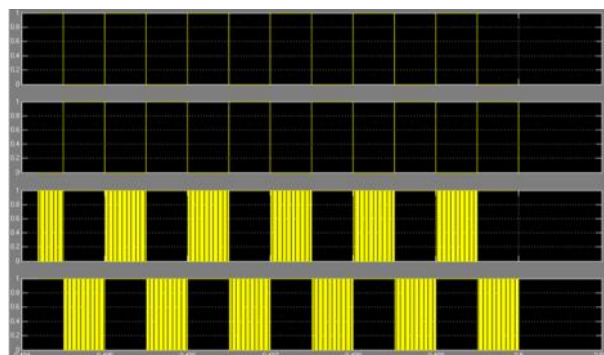


Fig.8 Control Strategy Of Proposed Converter

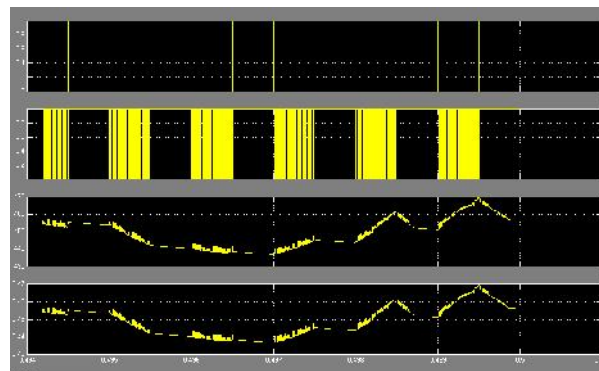


Fig.9 Some selected waveforms for simulation at full-load $P_o = 200\text{ W}$ and $V_{in} = 48\text{ V}$ of S_{c1}, S_{m1}, V_o, I_L

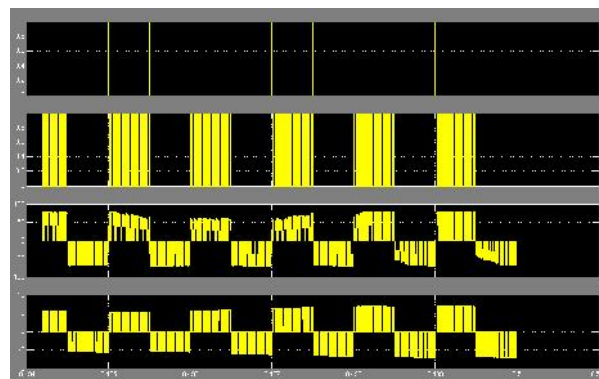


Fig.10. Some selected waveforms for simulation at full-load $P_o = 200\text{ W}$ and $V_{in} = 48\text{ V}$ of S_{c1}, S_{m1}, V_r, I_r

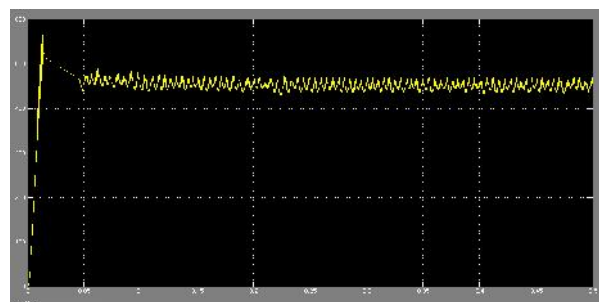


Fig. 11 Voltage (V_o)

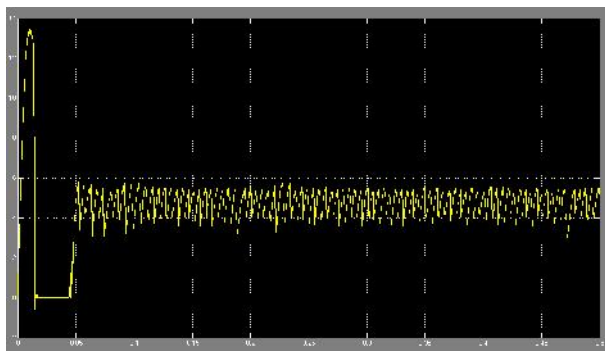


Fig. 12 Current I Inv

V. Conclusion

In my paper, got a high voltage gain and devoid of using Step up transformer through a high step-up DC-DC converter based on Cockcroft-Walton (CW) voltage multiplier. Since the voltage stress on the active switches, diodes, and capacitors is not affected by the number of cascaded stages, power components with same voltage ratings can be selected. The mathematical modeling, circuit operation, design considerations, and control strategy were discussed. The control strategy of the proposed converter can be easily implemented with a commercial average-current-control and continuous current mode with adding a programmed. The proposed control strategy employs two independent frequencies, one of which operates at high frequency to minimize the size of the inductor, while the other one operates at relatively low frequency according to the desired output voltage ripple. Finally, the simulation and experimental results proved the validity of theoretical analysis and the feasibility of the proposed converter. In future work, the influence of loading on the output voltage of the proposed converter will be derived for completing the steady-state analysis. Thus the design, simulation and analysis of proposed DC-DC boost converter with seven-stage Cockcroft Walton voltage multiplier was done.

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