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Supervision of DC Link Pi Control In A D-Statcom Based on Fuzzy Logic

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Abstract:-

PI controller with control algorithms are used for load compensation and voltage regulation in D-STATCOM. Because of variation in dc capacitor voltage, load changes might affect the compensation. In this paper, a fuzzy logic based supervisory method is proposed to improve the transient performance of the dc link. Proportional and integral gains of the PI controller varies the transient period time immediately after the load variation. PI gains using expert knowledge of system behavior and higher sampling during the transient period improves the performance of the controller. Error in dc link reduces capacitor voltage during load change compared to normal PI controller. Efficiency and settling time of voltage is also fast, will be proved using this proposed approach with MATLAB simulation results.

Keywords:-DC link voltage control, DSTATCOM, Fuzzy supervisor, PI controller, transient response, VSI.

1. INTRODUCTION:

Non-linear loads and the propagation of power electronic based equipment have led to many problems in the power distribution network. Solid state switching devices such as thyristors and other switches are used in UPS, batteries, variable speed drives etc. Because of their inherent non-linearity, they draw more reactive power and harmonic current components from the system. This affects the system efficiency, power factor and harmonic pollution of the system. Many power quality problems usually occur in the distribution system because of above problems. Harmonics and non-linear loads affect the quality of power received by the customers. Low power factor loads can cause power losses at the distribution feeder. The utility system does not have any control over the loads. This predictable approach to this solution has been the use of passive power filters. Though they are a low-cost solution, there are disadvantages to using them, the main problem being that of resonance with the system impedance. They are also bulky and overcompensation can affect the power factor. Distribution Static Compensator or the DSTATCOM is a shunt connected active power filter or conventional power device which injects current at the point of common coupling (PCC). The main aims of the DSTATCOM are:

a) To reduce the effect of harmonics due to load so that the current drawn from the source is nearly sinusoidal.

b) To facilitate maintaining the power factor near unity by reducing the effect of poor load power factor.

c) To help the offset effect of unbalanced loads such that the current drawn from the source is balanced. Various control algorithms have been proposed in this paper to absorb the reference currents of the compensator.

The theory of instantaneous symmetrical components has been used because of its simplicity in formulation and ease of calculation. The source voltages are assumed to be balanced sinusoids and stiff. The reference currents based on this theory are given in (1) below.

$$i_{fa}^{*} = i_{la} - i_{sa} = i_{la} - \frac{v_{sa} + \gamma(v_{sb} - v_{sc})}{(P_{lavg} + P_{loss})}$$

$$i_{fb}^{*} = i_{lb} - i_{sb} = i_{lb} - \frac{v_{sb} + \gamma(v_{sc} - v_{sa})}{(P_{lavg} + P_{loss})} \quad (1)$$

$$i_{fc}^{*} = i_{lc} - i_{sc} = i_{lc} - \frac{v_{sc} + \gamma(v_{sa} - v_{sb})}{(P_{lavg} + P_{loss})}$$

For obtaining unity power factor at the source, φ=0 and thus γ=0. The term 'P_{lavg}' is the average value of load power which would be a constant value if there is no load change. This is computed using a moving average filter for half cycle. 'P_{loss}' is the amount of

power that is required to be drawn from the source to compensate for the losses which occur in the inverter. So losses will be supplied by the dc capacitor and dc link voltage will drop. It is however very difficult to compute the exact losses that occur in the inverter. Thus, 'P_{loss}' is obtained using a PI controller. At steady state, the P_{loss} value is updated every half cycle or every 180 degrees. The sum of P_{loss} and 'P_{lavg}' terms determines the amount of power drawn from the source.

The moving average filter used to calculate *Plavg* takes half a cycle to settle to the new value of average power. During this time, the power to the load is supplied temporarily from the DSTATCOM. This leads to a decrease in dc link voltage if the load is increased or an increase in capacitor voltage if the load is reduced. For good compensation, it is important that the capacitor voltage remains as close to the reference value as possible. After a load change has occurred, depending on the values of K_P and K_i, the capacitor voltage takes 6-8 cycles to settle. Most of the times, the gains are chosen by trial and error method. A technique to obtain good K_P and K_i values for the DSTATCOM application is given in this strategy. This has been used as the base values during steady operation.

In this paper, it has been shown that fuzzy logic based supervision of the dc link PI controller gains improves the transient and settling performance of dc link voltage control. Hence, the use of fuzzy logic for this application is justified. This paper has been organized in the following manner. First an explanation of the VSI topology for the D-STATCOM used is given and then the state space modeling used to simulate the working of the D-STATCOM is explained. The design of the fuzzy supervisor for this system is elucidated. The methodology and results of the simulation are shown in the final section, proving improved dc link performance.

II. H-BRIDGE VSI TOPOLOGY BASED DSTATCOM:-

Many voltage source inverter (VSI) topologies have been used for DSTATCOM applications. The three phase H-bridge VSI topology has been chosen because of the presence of a single dc link capacitor (unbalance in capacitor voltages which may occur in topologies with two dc capacitors need not be considered), simplicity and independent current tracking in each phase. Fig. 1 shows a three phase, four wire compensated system using H-bridge VSI based DSTATCOM.

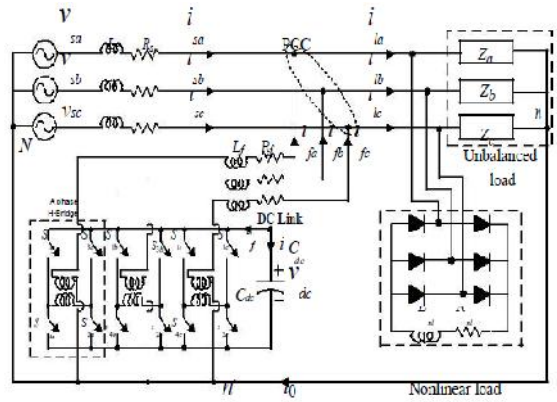

Fig. 1. A Three phase, four wire compensated system using H-bridge VSI based DSTATCOM.

The unbalanced and non-linear load used is also shown in the figure. The DSTATCOM has 12 IGBT switches with anti parallel diodes (not shown in the figure for the sake of clarity), a dc storage capacitor, three isolation transformers and three interface inductors. In modeling the system, the inductance and resistance of the isolation transformers can be included in *Lf* and *Rf*, the interface inductance and resistance. Since we assume the source voltages to be balanced, sinusoidal and stiff, *Ls* and *Rs*, the source impedances, are assumed to be negligible. Hysteresis band current control has been used for tracking the reference currents. As seen in Fig. 1, the DSTATCOM injects the reference filter currents generated using the symmetrical component theory at the Point of Common Coupling (PCC). For good current injection and thus compensation, maintaining the dc capacitor value close to the reference value is very important.

III. DC LINK PI CONTROL AND FUZZY SUPERVISION:-

During load changes, there is some active power exchange between the DSTATCOM and the load. This leads to a reduction or an increase in the dc capacitor voltage. Using a PI controller, the *Ploss* term in (1) is controlled to ensure that the dc capacitor voltage does not deviate from the reference value. The control output of a PI controller is given by (2).

$$P_{loss} = K_p (v_{dc}^{ref} - v_{dc}) + K_i \int (v_{dc}^{ref} - v_{dc})\, dt \qquad (2)$$

The input to the PI controller is the error in the dc link voltage and the output is the value of P_{loss}. The value of P_{loss} depends on the value of K*p*, *Ki* and the error in dc link voltage. Thus, it is important to tune *Kp* and *Ki* properly. Because of the inherent non-linearity and complexity of the system, it is difficult to tune the gains of the controller. It is usually done by trial and error. The base values of *K p* and *Ki* have been designed using the energy concept proposed in. Also, it has been shown in literature that fuzzy supervision can improve the performance of PID controllers in nonlinear systems.However, these mostly deal with set-point changes in control applications. The derivative control term is not used because improvement in stability may or may not be obtained when used only with proportional control and if it is used with integral control as well, tuning for good performance is difficult [13]. The design of a fuzzy system is highly system specific and requires in-depth knowledge of the system and the various parameters that can be controlled for good performance. The design of a fuzzy supervisor for dc link PI control in a DSTATCOM is given in the next section.

IV. DESIGN OF THE FUZZY LOGIC SUPERVISOR FOR PI CONTROLLER:-

PID controllers are extensively used in industry for a wide range of control processes and provide satisfactory performance once tuned when the process parameters are well known and there is not much variation. However, if operating conditions vary, further tuning may be necessary for good performance. Since many processes are complicated and nonlinear, fuzzy control seems to be a good choice. Literature shows many approaches where the PI controller has been replaced by a fuzzy controller. However, instead of completely modifying the control action, it is sufficient to use an additional level of control by supervising the gains using fuzzy techniques to improve the performance of the system.

A PI controller is preferred to regulate the dc link voltage as the presence of the integral term ensures zero steady state error. The dc link capacitor voltage waveform contains a ripple because according to the instantaneous symmetrical component theory, which is used in this work, the compensator supplies the oscillating part of the active power also. Thus there is always a zero average oscillating power exchange between the compensator and the load. This ripple can be seen in the simulation results in Fig. 9. The fuzzy controller scaling has been designed to give a good output irrespective of the presence of the ripple during the transient period.

Some of the main aspects of fuzzy controller design are choosing the right inputs and outputs and designing each of the four components of the fuzzy logic controller shown in Fig. 2. Each of these will be discussed in the subsections below: Also, the fuzzy controller is activated only during the transient period and once the value of the dc link voltage settles down, the controller gains are kept constant at the steady state value.

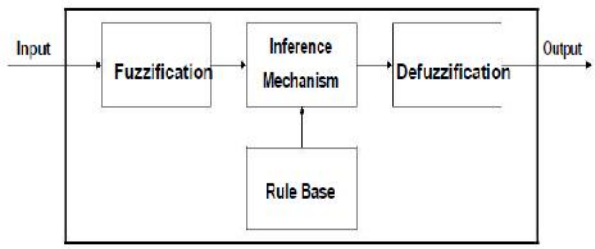

Fig. 2: Fuzzy controller architecture.

A. Inputs and Outputs:

The inputs of the fuzzy supervisor have been chosen as the error in dc link voltage and the change in error in dc link voltage.

$$err(i) = v_{dc}^{ref} - v_{dc}(i) \qquad (3)$$

$$derr(i) = err(i) - err(i-1) \qquad (4)$$

In (3) and (4) above, e(i) is the error and *e*(*i*) is the change in error in the ith iteration. Vdc^{ref} *ref* is the reference dc link voltage and *vdc* (*i*) is the dc link voltage in the ith iteration. The outputs of the fuzzy supervisor are chosen as the change in *Kp* value and the change in *Ki* value.

$$K_P = K_{P\,ref} + K_P \qquad (5)$$

$$K_i = K_{i\,ref} + K_i \qquad (6)$$

And $K_{i\,ref}$ are the steady state values determined by the method specified in [7]and *Kp* and *Ki* are the outputs of the fuzzy logic supervisor.

B. FUZZIFICATION:-

The fuzzification interface modifies the inputs to a form in which they can be used by the inference mechanism. It takes in the crisp input signals and assigns a membership value to the membership function under whose range the input signal falls. Typical input membership functions are triangular trapezoidal or exponential. Seven triangular membership functions have been chosen: *NL* (Negative Large), *NM* (Negative Medium), *NS* (Negative Small), *Z* (Zero), *PS* (Positive Small),

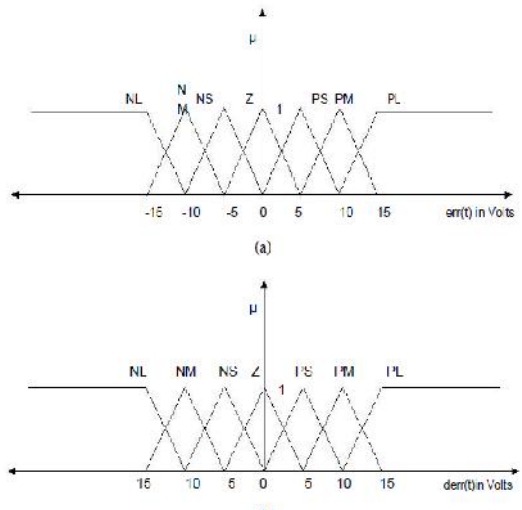

Fig.3(a): Membership functions for error input. (b) Membership functions for change in error input

PM (Positive Medium) and *PL* (Positive Large) for both error (*err*) and change in error (*derr*) . The input membership functions are shown in Fig. 3. The tuning of the input membership function is done based on the requirement of the process. Each membership function has a membership value belonging to [0 1]. It can be observed that for any value of error or change in error, either one or two membership functions will be active for each.

C. Inference Mechanism:-

The two main functions of the inference mechanism are:

a) Based on the active membership functions in error and the change in error inputs, the rules which apply for the current situation are determined.
b) Once the rules which are on are determined, the certainty of the control action is ascertained from the Membership values. This is known as premise quantification.

Thus at the end of this process, we shall have a set of rules each with a certain certainty of being valid. The database containing these rules is present in the rule base from which the control action is obtained. The rule base will be discussed in the next section. An example of a rule is given in (7). He terms *PL* and *PM* are the membership functions for error and for change in error respectively.

IF
"*Error*" is *PL* (positive large)
"*Change in error*" is *PM* (positive medium)
(7)
THEN
"Kp" is *L* (Large Kp)
"Ki" is *S ki* (Small Ki)

The minimum operation is used to determine the certainty called μ premise of the rule formed by their combination.

D. The Rule Base:-

Designing the rule base is a vital part in designing the Controller. It is important to understand how the rule base has been designed. Fig. 4 shows a typical dc link voltage waveform after an increase in the load without the inherent ripple due to compensation. The waveform has been split into various parts depending on the sign of error and change in error.

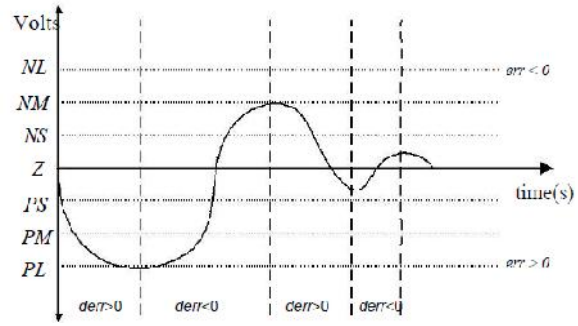

Fig. 4: Typical dc link voltage waveform after a load change.

The rules in the rule base are designed based on which part of the graph the waveform is in. The important points involved in the design of the rule base are the following:

a) If the error is large and the change in error shows the dc link waveform deviating away from the reference, then increase *KP*.
b) If the waveform is approaching the reference value, then increase the *Ki* value to reduce overshoot

and improve settling time. Keeping these aspects in mind, two rule base matrices have been developed for *Kp* and *Ki*. Fig. 5(a) gives the rule base matrix for *Kp* and Fig. 5(b) gives the rule base matrix for *Ki*. The output membership functions for the proportional gain are *LKi*, *SKi* and *Z* and the output membership functions for integral gain are *L*, *M*, *S* and *Z*. These matrices provide rules such as the example seen in (7) for all possible combinations of the membership functions for error and change in error. Thus, using information from the rule base, the rule and its certainty is determined by the inference mechanism. The method to convert the fuzzy result to crisp control action is called defuzzification. This is explained in the next section.

derr / err	NL	NM	NS	Z	PS	PM	PL
NL	L	L	L	M	S	S	Z
NM	L	L	M	S	S	Z	S
NS	L	M	S	S	Z	Z	Z
Z	M	Z	Z	Z	Z	Z	M
PS	Z	Z	Z	S	S	M	L
PM	S	Z	S	S	M	L	L
PL	Z	S	S	M	L	L	L

(a)

derr / err	NL	NM	NS	Z	PS	PM	PL
NL	SK_i	SK_i	SK_i	Z	Z	Z	Z
NM	SK_i	SK_i	SK_i	Z	Z	Z	Z
NS	LK_i	LK_i	LK_i	Z	Z	Z	Z
Z	LK_i	LK_i	LK_i	Z	LK_i	LK_i	LK_i
PS	Z	Z	Z	Z	LK_i	LK_i	LK_i
PM	Z	Z	Z	Z	SK_i	SK_i	SK_i
PL	Z	Z	Z	Z	SK_i	SK_i	SK_i

(b)

Fig. 5(a) Rule base matrix for change in *Kp*. (b) Rule base matrix for change in *Kp*

E. Defuzzification:

The inference mechanism provides us with a set of rules each with a *µpremise*. The defuzzification mechanism considers these rules and their respective *µpremise* values, combines their effect and comes up with a crisp, numerical output. Thus, the fuzzy control action is transformed to a non fuzzy control action. The 'center of gravity' method has been used in this work for this. If we use this method, the resultant crisp output is sensitive to all of the active fuzzy outputs of the inference mechanism. Fig. 6(a) and Fig. 6(b) show the output membership functions chosen for *Kp* and *Ki*.

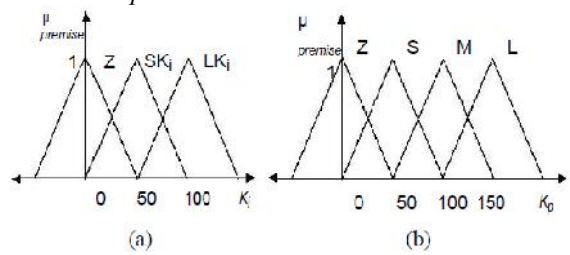

Fig. 6(a): Output membership function for *Kp* (b) Output membership function *Ki.*

According to this method the weighted mean of the center values of the active output membership functions is taken as the output, the weights being the area under the line representing the *µpremise*.

V. SIMULATION STUDY AND RESULTS

Fig. 1 shows the compensated system using a H-bridge VSI based DSTATCOM. This has been simulated in MATLAB. All switches shown in Fig.1 are considered ideal. The ac load is a three phase unbalanced load and a three phase diode bridge rectifier feeding an inductive R-L load. The parameters of the system are given in Table 1. Since the average load power is supplied by the source, the following holds true.

$$V_{sa}\, i_{la} + V_{sb}\, i_{lb} + V_{sc}\, i_{lc} = P_{lavg} \qquad (6)$$

To compute *Plavg* a moving average filter for half a cycle has been used. In steady state, at each zero crossing of the phase *a* voltage, *Ploss* is generated using the PI controller.

TABLE I
SIMULATION PARAMETERS

System Parameters	Values
Supply voltage	220V (phase rms), 50 Hz
Unbalanced load	$R_{la} = 50\ \Omega$, $L_{la} = 20$ mH $R_{lb} = 35\ \Omega$, $L_{lb} = 40$ mH $R_{lc} = 70\ \Omega$, $L_{lc} = 20$ mH
Non-linear load	Three-phase full wave rectifier drawing a dc current of 5 A
DC capacitor	$C_{dc} = 2200\ \mu F$
Interface inductor	$L_f = 20$ mH, $R_f = 5\ \Omega$
Reference dc link voltage	$V_{dc\,ref} = 500$ V
Hysteresis band	$h = 0.6$ A
Arbitrarily tuned controller gains	$K_p = 40$, $K_i = 20$
Gains tuned using the Energy concept	$K_p = 110$, $K_i = 55$

The state space modeling of the system shown in Fig.1. Has been used to compute the state variables i.e. the actual compensator currents and the dc link voltage. Details of the state space modeling and analysis of the DSTATCOM can be obtained from. These compensator currents are then compared to the reference currents generated using the symmetrical component theory as given by (1). Then, Hysteresis current control is used to determine the next switching state of the switches in the VSI. During the transient state after load change, however, faster sampling at every 45 degrees is done for dc voltage control and the fuzzy supervisor is activated to ensure that the dc capacitor voltage quickly returns close to the reference value.

The source voltages and the load currents have been plotted in Figs. 7(a)-(b). The load consists of an unbalanced R-L load and a diode rectifier supplying a highly inductive load as given in Table 1. The THDs for the load currents for phase *a*, phase *b* and phase *c* are 12.3%, 10.5% and 14.5% respectively. Phase-*a* compensator current showing the hysteresis action is shown is shown in Fig. 8(a) and the compensated source currents are shown in Fig. 8(b).

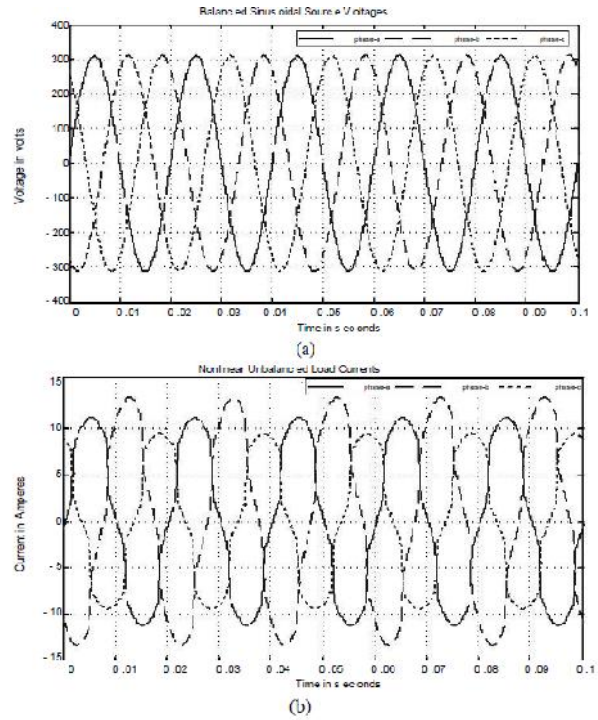

Fig. 7(a). Balanced sinusoidal source voltages (b) Nonlinear unbalanced load currents.

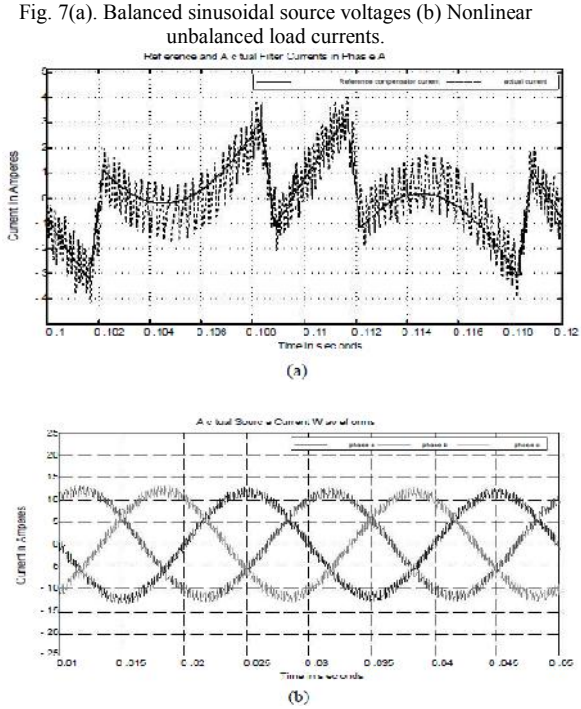

Fig. 8(a): Phase-a reference and actual compensator currents (b) Balanced and sinusoidal source currents.

The source currents have a unity power factor and are balanced sinusoids. The THDs for the source currents for phase *a*, phase *b* and phase *c* are 1.63%, 1.77% and 1.58% respectively. Thus, we can

clearly observe the compensating action of the DSTATCOM. Fig. 9 shows the voltage waveforms when a normally tuned PI (using the fast acting dc concept[7]) and a fuzzy supervised PI controller are used. Clearly, the fuzzy PI controller gives a better performance of the dc link with lesser settling time and nearly 50% lesser deviation of the dc link during load change. The load has been doubled at 0.2 seconds and at 0.4 seconds, it is brought back to the original value. A clear dip in the dc link voltage is seen at 0.2 seconds as the compensator supplies the load during the transient period after the increase in load.

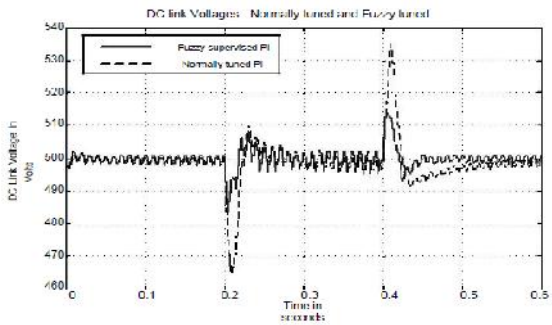

Fig. 9. DC link voltages using fuzzy supervised and normally tuned PI controllers.

An increase in voltage at 0.4 seconds when the compensator takes power from the load during the transient period after the load has been brought back to the initial value. From Fig. 9, we clearly see an improvement in dc link performance.

VI. CONCLUSIONS

DSTATCOM based fuzzy logic supervisor to the dc link PI controller has been proposed in this paper. System performance can be improves by the supervisor, varies the gain of the PI controller during the transient period. The system has been modeled and simulated in the MATLAB. The performance of the dc link and compensation were observed with and without the fuzzy supervisor. Simulation results show a 50% reduction in voltage deviation of the dc link voltage with faster settling time. Instantaneous symmetrical component theory has been used for load compensation. Good compensation has been observed as source current THDs for each phase is 1.63%, 1.77% and 1.58% while the load THDs are 12.37%, 10.5% and 14.54% respectively. Thus, through simulation studies, the implementation of a fuzzy supervisor for DC link voltage control in a DSTATCOM using instantaneous symmetrical component theory for load were observed.

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