International Journal of Science Engineering and Advance Technology

Power Quality Improvement In Distribution Systems Using Facts Devices

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ABSTRACT:

The quality of available supply power has a direct economic impact on industrial and domestic sectors which affects the growth of any nation.This paper proposes an algorithm to produce reference voltage for a distribution static compensator (DSTATCOM) working in voltage-control mode. The proposed plot displays a few favorable circumstances contrasted with customary voltage-controlled DSTATCOM where the reference voltage is subjectively taken as 1.0 p.u. The proposed plot guarantees that unity power factor (UPF) is accomplished at the heap terminal amid ostensible operation, which is unrealistic in the customary technique. Additionally, the compensator infuses bring down currents and, hence, reduces losses in the feeder and voltage-source inverter. Advance, a sparing in the rating of DSTATCOM is accomplished which builds its ability tomitigate voltage sag. About UPF is kept up, while managing voltage at the load terminal, amid load change. The state-space model of DSTATCOM is consolidated with the deadbeat prescient controller for quick load voltage direction amid voltage unsettling influences. With these components, this plan permits DSTATCOM to handle control quality issues by giving power factor correction, consonant disposal, stack adjusting, and voltage direction in view of the load prerequisite.

KEYWORDS: Current control mode, power quality (PQ), voltage-control mode, voltage-source inverter.

I. INTRODUCTION:

In voltage-control mode (VCM), the DSTATCOM manages PCC voltage at a reference esteem to shield basic burdens from voltage unsettling influences, for example, list, swell, and unbalances. Be that as it may, the upsides of CCM and VCM can't be accomplished at the same time with one dynamic channel gadget, since two modes are autonomous of each other. In CCM operation, the DSTATCOM can't adjust for voltage unsettling influences. Henceforth, CCM operation of DSTATCOM is not helpful under voltage aggravations, which is a noteworthy disservice of this method of operation. Customarily, in VCM operation, the DSTATCOM controls the PCC voltage at 1.0 p.u.. In any case, a heap works attractively for an admissible voltage go. Thus, it is not important to direct the PCC voltage at 1.0 p.u. While keeping up 1.0-p.u. voltage, DSTATCOM makes up for the voltage drop in feeder. For this, the compensator needs to supply extra receptive streams which builds the source ebbs and flows. This builds misfortunes in the voltage-source inverter (VSI) and feeder. Another vital perspective is the rating of the VSI. Because of expanded current infusion, the VSI is de-evaluated in consistent state condition. Thus, its ability to relieve profound voltage list diminishes. Additionally, UPF can't be accomplished when the PCC voltage is 1 p.u. In the writing, as such, the operation of DSTATCOM is not reported where the benefits of both modes are accomplished in light of load necessities while conquering their faults.

LITERATURE SURVEY:

THE AUTHOR,Chandan Kumar and **Mahesh K. Mishra (ET .AL),AIM IN** a new algorithm to generate reference voltage for a DSTATCOM operating in voltage-control mode. The proposedscheme exhibits several advantages compared to traditional voltage-controlled DSTATCOM where the reference voltage is arbitrarily taken as1.0 p.u. The proposed scheme ensures that unity power factor is achieved at the load terminal during nominal operation, which is not possible in the traditional method.

THE AUTHOR, A. Ghosh**(ET .AL), AIM IN** a load pay methods under lopsided and distorted voltages have been talked about. Two sorts of compensation strategies are considered. In the main class, synchronous recognition and adjusted equivalent current techniques are utilized under the unequal however sinusoidal source voltages. To bolster the proposed strategy, a 440 V (L-L) three-stage, four-wire appropriation framework is considered.

THE AUTHOR,M. K. Mishra **(ET .AL), AIM IN**the working standards of an appropriation static compensator (DSTATCOM) that is utilized to keep up the voltage of a conveyance transport. A three-stage, four-wire appropriation framework is accepted in this study. The extent of the transport voltage is picked as ostensible esteem, i.e., 1.0 p.u., while its

stage point is gotten through a criticism circle that keeps up the voltage over the dc stockpiling capacitors. Through point by point simulation and test comes about, it has been demonstrated that the DSTATCOM can keep up the voltage against any unbalance and contortion in either the heap or supply side.

PROBLEM DEFINITION

The DSTATCOM can't adjust for voltage unsettling influences. Subsequently, CCM operation of DSTATCOM is not helpful under voltage aggravations, which is a noteworthy burden of this method of operation. Generally, in VCM operation, the DSTATCOM manages the PCC voltage at 1.0 p.u.. Be that as it may, a load works attractively for an allowable voltage go. Subsequently, it is not important to manage the PCC voltage at 1.0 p.u. While keeping up 1.0-p.u. voltage, DSTATCOM adjusts for the voltage drop in feeder.

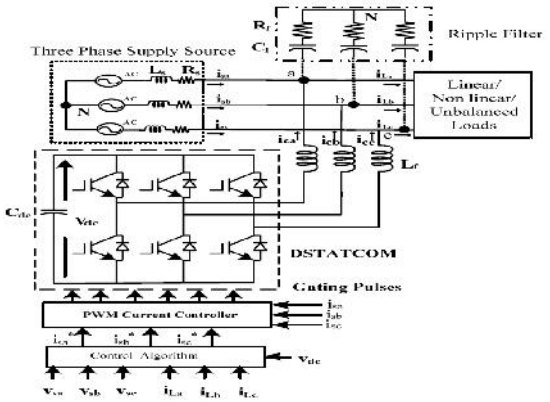


Fig.1:Existing DSTATCOM.

PROPOSED APPROACH

The operation of DSTATCOM in VCM and proposes a control calculation to acquire the reference stack terminal voltage. This calculation gives the consolidated favorable circumstances of CCM and VCM. The UPF operation at the PCC is accomplished at ostensible load, though quick voltage control is given amid voltage unsettling influences. Likewise, the receptive and consonant part of load current is provided by the compensator whenever of operation. The bum prescient controller is utilized to produce exchanging beats. The control technique is tried with a three-stage four-wire appropriation framework.

PROPOSED METHOD:

CIRCUIT DIAGRAM OF THE DSTATCOM-COMPENSATED IN DISTRIBUTION SYSTEM.

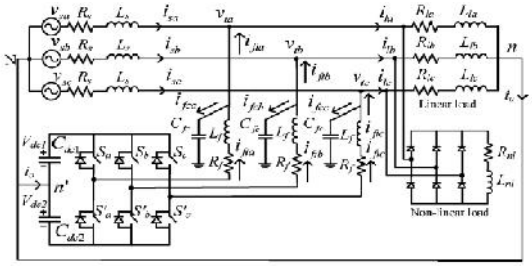


Fig.2:Three-phase equivalent circuit of DSTATCOM.

SINGLE-PHASE EQUIVALENT CIRCUIT OF DSTATCOM:

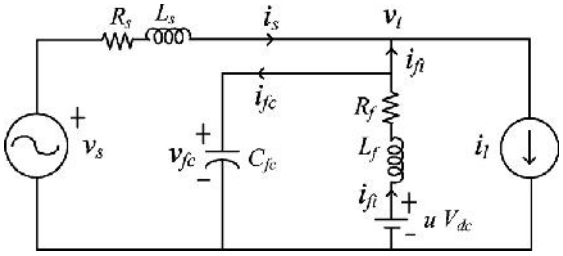


Fig.3:Single-phase equivalent circuit of DSTATCOM.

PROPOSED CONTROL SCHEME:

The PCC voltage can be regulated to the desired value with properly chosen parameters of the VSI. A proportional-integral (PI) controller is used to regulate the dc capacitor voltage at a reference value. Complex Fourier transform is used to reference voltage magnitude generation scheme is proposed that provides the advantages of CCM at nominal load.

System Modeling and Generation of the Voltage-Control Law:

The state-space equations for the circuit shown in Fig.3 are given

$$x^* = Ax + Bz \quad \text{.....(1)}$$

By applying KVL to the Figure 3

$$v_s = L_s \frac{di_s}{dt} + R_s i_s + v_l \quad \text{.....(2)}$$

$$UV_{dc} = L_f \frac{di_f}{dt} + R_f i_f + V_{fc} \quad \text{.....(3)}$$

By applying KCL to the Figure 3

$$C_{fc} \frac{dV_{fc}}{dt} + i_{ft} + i_{fi} = 0 \quad \text{.....(4)}$$

- The general time-domain solution of (1) to compute the state vector x(t) with known initial value x(t0), is given as follows:

$$\mathbf{(t)}=e^{A(t-t_0)}\mathbf{X(t0)}+\int_{t_0}^{t} e^{A(t-T)}\boldsymbol{Bz}(T)dT$$

……(5)

- The equivalent discrete solution of the continuous state is obtained by replacing **t0 = kTd**and **t = (k+1)Td** as follows:

$$\mathbf{X(K+1)}=e^{A(T_d)}\mathbf{X(k)}+\int_{kT_d}^{(K+1)T_d} e^{A(T_d+kT_d-T)}\boldsymbol{Bz}(T)dT$$

…… (6)

- In equation(6), K = K^{th} sample and Td = sampling period.
- During consecutive sampling period, the value of$z(T)$ is held constant, and can be taken as $z(K)$.

Equation (6) can be written as

$$\mathbf{X(K+1)}=e^{A(t_d)}\mathbf{X(k)}+\int_{kT_d}^{(K+1)T_d} e^{A(T_d+kT_d-T)}\boldsymbol{Bz}(T)dT$$

… (7)

- Equation (7) is rewritten as follows:

$$x(K+1)=Gx(k)+Hz(K) \quad \text{… (8)}$$

- Where G and H are sampled matrices, with a sampling time of T_d. For small sampling time, matrices G and H are calculated as follows:

$$G=\begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d}=I+AT_d+\frac{(AT_d)^2}{2}\ldots.(9)$$

$$H=\begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda}Bd\lambda = \int_0^{T_d}(1+A\lambda)Bd\lambda \ldots.(10)$$

- Hence the capacitor voltage using (5) is given as

$$V_{fc}(k+1) = G_{11}V_{fc}(k)+G_{12}i_{fi}(k)+H_{11}u(k)+H_{12}i_{ft}(k)$$

….(11)

Here therefore, VSI parameters must be chosen carefully.

- A cost function J is chosen as follows

$$J = [V_{fc}(k+1)- V_t^*(k+1)]^2 \quad \text{……(12)}$$

- The cost function is differentiated with respect to u(k) and its minimum is obtained at

$$V_{fc}(k+1)=V_t^*(k+1)\text{……(13)}$$

- The deadbeat voltage-control law, from equations (11) and (13),is given as

$$U^*(k) = \frac{V_t^*(k+1)-G_{11}V_{fc}(k)-G_{12}i_{fi}(k)-H_{12}i_{ft}(k)}{H_{11}}$$

……..(14)

- Using One-step-ahead prediction of this voltage is done using a second-order Lagrange extrapolation formula as follows

$$V_t^*(k+1)=3\,V_t^*(K) - 3\,V_t^*(K\text{-}1)\,3+ V_t^*(K\text{-}2)$$

……..(15)

- Finally, $u^*(K)$ is converted into the ON/OFF switching command to the corresponding VSI switches using a deadbeat hysteresis controller.

DESIGN OF VSI PARAMETERS:

- DSTATCOM regulates terminal voltage satisfactorily, depending upon the properly chosen VSI parameters.
- Voltage Across DC Bus (Vdc): The dc bus voltage is taken twice the peak of the phase voltage of the source for satisfactory performance. Therefore, for a line voltage of 400 V, the dc bus voltage is maintained at 650 V.

$$Vdc=\frac{2\sqrt{2}}{\sqrt{3}}*VLL \quad \text{……..(16)}$$

DC capacitance (cdc):

- Values of dc capacitors are chosen based on a period of sag/swell and change in dc bus voltage during transients.
- In the worst case, the load power may vary from minimum to maximum that is from 0 to S kVA.
- The compensator needs to exchange real power during transient to maintain the load power demand.
- This transfer of real power during the transient will result in the deviation of capacitor voltage from its reference value.
- Consider voltage controller takes p cycles, pT seconds to act,

Where T is the system time period.

- Hence, maximum energy Exchange by the compensator during transient will be pST.
- This energy will be equal to the change in the capacitor stored energy. Therefore

$\frac{1}{2}$cdc (V$dcref^2$ − Vdc^2) = pST …..(17)

Cdc = $\frac{2pST}{(Vdcref^2-Vdc^2)}$…..(18)

- Filter inductance(Lf): Filter inductance Lf should provide reasonably high switching frequency and a sufficient rate of change of current such that VSI currents follow desired currents.
- The following equation represents inductor dynamics:

$$L_f \frac{di_{fi}}{dt} = -v_{fc} - R_f i_{fi} + V_{dc} \text{.....(19)}$$

- The inductance is designed to provide good tracking performance at a maximum switching frequency which is achieved at the zero of the source voltage in the hysteresis controller.
- Neglecting R_f, L_f is given by

$$L_f = \frac{2V_m}{(2h_c)(2f_{max})} = \frac{0.5V_m}{h_c f_{max}} \text{.....(20)}$$

- Shunt Capacitor : The shunt capacitor should not resonate with feeder inductance at the fundamental frequency. Capacitance, at which resonance will occur, is given as

$$C_{fcr} = \frac{1}{\omega_0^2 L_s} \quad \text{……(21)}$$

Controller for DC Bus Capacitor Voltage:

Average real power balance at the PCC will be P_{pcc}, P_{lavg}, *and* P_{loss} are the average PCC power, load power, and losses *in the* VSI, respectively.

The power available at the PCC, which is taken from the source, depends upon the angle between source and PCC voltages, that is, load angle δ.

Henceδ, must be maintained constant to keep PCC constant.

$\delta = K_{p\delta}\, e_{vdc} + K_{i\delta} \int e_{vdc}\, dt$ ……(22)

Where

$e_{vdc} = 2V_{dcref} - (V_{dc1} + V_{dc2})$ ……(23)

is the voltage error Terms.

$K_{p\delta}$ *and* $K_{i\delta}$ are proportional and integral gains.

δ *must lie between* 0 *to* 90 *for the power flow from source*

to PCC. Hence controller gains must be chosen carefully

Proposed Method To Generate Reference Terminal Voltages

$i_{ij}(t) = \sum_{n=1}^{m} \sqrt{2}\, I_{ij} \sin(nwt + \emptyset_{ij})$ …(24)

j = a,b,c represent three phases

n = harmonic number

m = maximum harmonic order

$$\begin{bmatrix} i_{la}^0(t) \\ i_{la}^+(t) \\ i_{la}^-(t) \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \propto & \propto^2 \\ 1 & \propto^2 & \propto \end{bmatrix}\begin{bmatrix} i_{la}(t) \\ i_{la}(t) \\ i_{la}(t) \end{bmatrix}$$

where $\propto = e^{j2\pi/3}$

- The fundamental positive-sequence component of load current, calculated by finding the complex Fourier coefficient, is expressed as follows

$$\bar{I}_{la}^+(t) = \frac{\sqrt{2}}{T}\int_0^T i_{la}^+(t)\, e^{-j(wt-90)} dt \quad \text{……(25)}$$

$$\bar{I}_{la1}^+ = |\bar{I}_{la1}^+| \angle \bar{I}_{la1}^+ \text{ ……(26)}$$

$$\bar{\imath}_{la1}^{-+}(t) = \sqrt{2}\,\left|\bar{I}_{la}^+\right| \sin(wt + \angle \bar{I}_{la1}^+) \text{ ……(27)}$$

$$i_{sa}^* = \bar{\imath}_{la1}^{-+}(t) = \sqrt{2}\,\left|\bar{I}_{la}^+\right| \sin(wt - \delta_0) \text{……(28)}$$

$$i_{sb}^* = \bar{\imath}_{lb1}^{-+}(t) = \sqrt{2}\,\left|\bar{I}_{lb1}^+\right| \sin(wt - \tfrac{2\pi}{3} - \delta_0) \text{……(29)}$$

$$i_{sc}^* = \bar{\imath}_{lc1}^{-+}(t) = \sqrt{2}\,\left|\bar{I}_{lc1}^+\right| \sin(wt + \tfrac{2\pi}{3} - \delta_0) \text{……(30)}$$

$$v_{tj}(t) = V_{sj}(t) - L_s \frac{di_{sj}^*}{dt} - R_s i_{sj}^* \text{ .....(31)}$$

$$v_{la}(t) = \sqrt{2}\, V_l^* \sin \omega t \text{ .....(32)}$$

$$i_{sa}^* = \sqrt{2}\,|\bar{I}_{la1}^+| \sin \omega t \text{ .....(33)}$$

$$v_{sa}(t) = \sqrt{2}\, V \sin(\omega t + \delta_0) \text{ .....(34)}$$

$$V_t^* \angle 0 = V \angle 0 - (R_s + j\, X_s)\, |\bar{I}_{la1}^+| \angle 0 \text{ .....(35)}$$

$$V_t^* \angle 0 = V\cos(\delta^0) + jV\sin(\delta^0) - |\bar{I}_{la1}^+| R_s - j|\bar{I}_{la1}^+| X_s$$

.....(36)

$$V\cos(\delta_0) = V_t^* + |\bar{I}_{la1}^+| R_s \quad \text{.....(37)}$$

$$V\sin(\delta_0) = |\bar{I}_{la1}^+| X_s \quad \text{.....(38)}$$

$$V_2 = (V_t^* + |\bar{I}_{la1}^+| R_s)^2 + (|\bar{I}_{la1}^+| X_s)^2 \quad \text{.....(39)}$$

$$v_t^* = \sqrt{V^2 - (|\bar{I}_{lb1}^+| X_s)^2} - |\bar{I}_{lb1}^+| R_s \quad \text{.....(40)}$$

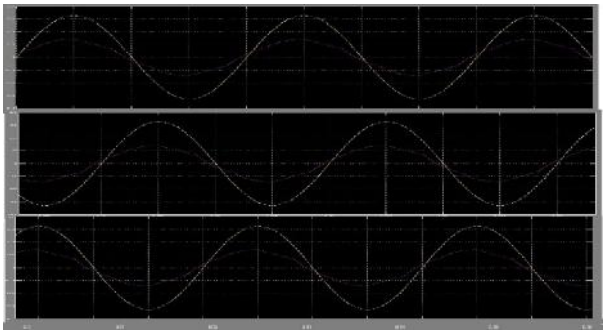
$$v_{ta}^*(t) = \sqrt{2}\, V_t^* \sin(wt - \delta_0) \quad \text{.....(41)}$$

$$v_{tb}^*(t) = \sqrt{2}\, V_t^* \sin(wt - \tfrac{2\pi}{3} - \delta_0) \quad \text{.....(42)}$$

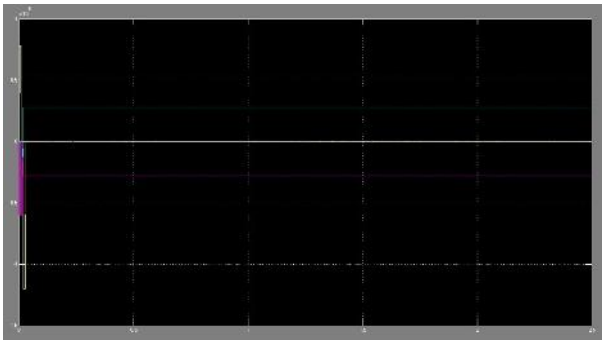
$$v_{tc}^*(t) = \sqrt{2}\, V_t^* \sin(wt + \tfrac{2\pi}{3} - \delta_0) \quad \text{.....(43)}$$

RESULTS:

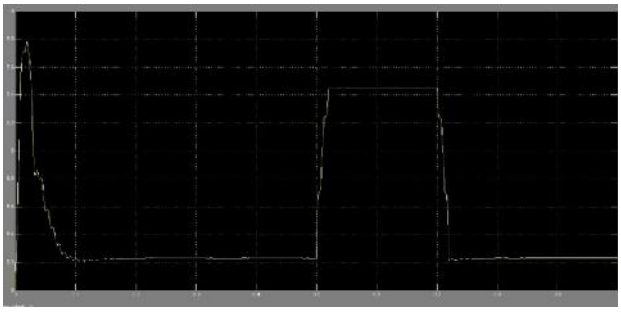
Terminal voltages and source currents using the proposed method.



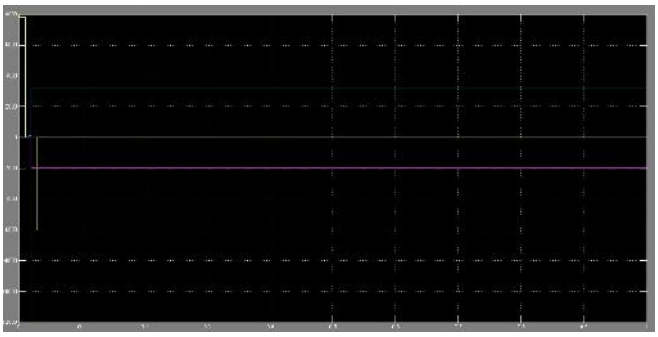
Load,compensator and PCC reactive powers in proposed method



Load angle in extension method



Reactive powers in extension method



CONCLUSION:

A control algorithm has been proposed for the era of reference load voltage for a voltage-controlled DSTATCOM. The execution of the proposed plan is contrasted and the customary voltage-controlled DSTATCOM. The proposed technique is superior to anything ostensible in taking after viewpoints like. At ostensible load, the compensator infuses receptive and symphonious segments of load streams, bringing about UPF. Almost UPF is kept up for a heap change. The execution of the UPQC is contrasted and the proposed voltage-controlled DSTATCOM. Quick voltage direction has been accomplished amid voltage aggravations and Losses in the VSI and feeder are diminished significantly and have higher hang supporting ability with similar VSI rating contrasted with the proposed conspire. The recreation comes about check that the proposed DSTATCOM and UPQC is capacity to enhance a few PQ issues (identified with voltage and current).

FUTURE WORK:

In this project dynamic, receptive power stream, three stage voltage and ebbs and flows of an irritated framework with DSTATCOM and UPQC gadget can watch better execution concerning the time reaction with FUZZY Logic set up of PI controllers. A power framework may contain unbalances, symphonious mutilation and even D.C. parts. The DSTATCOM and UPQC gadget can work with preferable time reaction over PI controllers, with every one of these perspectives keeping in mind the end goal to give shunt or arrangement compensation amid ordinary and fault conditions. Practical Swamping Algorithm (or) Ant Colony Search Method is utilized as a part of place of Dead Beat Predictive Control for better execution as for the time reaction, Reactive, Real power Loss and voltage Regulation.

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