International Journal of Science Engineering and Advance Technology

A New Multilevel Inverter Topology Based on Switched Capacitor for Power Quality Improvement

G Bhaskar Rao[1], G V Ram Mohan[2],D B Chowdary[3]
M.Tech Student, Department of EEE, KIET-II, Kakinada, India.[1]
Asst. Professor, Department of EEE, KIET-II, Kakinada, India.[2]
Asso. Professor, Department of EEE,RIET, Rajamundry, India.[3]

Abstract- The expansion of transmission frequency uncovers a larger number of benefits than low-or medium-frequency dissemination among various types of power applications. High-frequency inverter fills in as source side in high-frequency air conditioning (HFAC) power distribution system (PDS). Be that as it may, it is confused to get a high-frequency inverter with both basic circuit topology and clear modulation strategy. A novel switched capacitor-based fell multilevel inverter is proposed in this venture, which is developed by an exchanged capacitor frontend and H-Bridge backend. Through the change of series and parallel associations, the switched capacitor builds the quantity of voltage levels. The yield harmonic and the component counter can be fundamentally decreased by the expanding number of voltage levels. what's more, aggregate consonant mutilation is decreased in 17 and 13-level inverter when contrasted with 9-level inverter A symmetrical triangular waveform modulation is proposed with a basic simple usage and low regulation frequency contrasting and customary multicarrier tweak. Simulation results are introduced to check the attainability of the proposed approach in MATLAB/SIMULINK environment.

Index Terms—Cascaded H-Bridge, high-frequency ac (HFAC), multilevel inverter, switched capacitor (SC), symmetrical phase shift modulation (PSM).

INTRODUCTION

HIGH-FREQUENCY air conditioning (HFAC) power distribution system (PDS) possibly turns into an other option to conventional dc dissemination due to the less components and lower cost. The current applications can be found in PC [1], telecom [2], electric vehicle [3], and renewable vitality smaller scale lattice [4], [5]. Be that as it may, HFAC PDS needs to go up against the difficulties from expansive power limit, high electromagnetic obstruction (EMI), and serious power misfortunes [6]. A conventional HFAC PDS is comprised of a high-frequency (HF) inverter, a HF transmission track, and various voltage-control modules (VRM).HF inverter finishes the power transformation to suit the necessity of purpose of load (POL). So as to expand the power limit, the most well known strategy is to associate the inverter yield in series or in parallel. In any case, it is unreasonable for HF inverter, since it is convoluted to all the while synchronize both plentifulness and stage with HF flow. Multilevel inverter is a viable answer for increment control limit without synchronization thought, so the higher power limit is anything but difficult to be accomplished by multilevel inverter with lower switch push. No contaminated sinusoidal waveform with the lower add up to consonant twisting (THD) is basically brought on by long track conveyance in HFAC PDS. The higher number of voltage levels can adequately diminish add up to music substance of staircase yield, along these lines altogether rearranging the channel plan [7].HF control dissemination is appropriate for little scale and inside shut electrical system in electric vehicle (EV) because of direct size of dispersion system and powerful weight lessening [8]. The thought of operation frequency needs to make bargain between the air conditioner inductance and resistance [9], so multilevel inverter with the yield frequency of around 20 kHz Isa practical trial to fill in as power hotspot for HF EV application. The conventional topologies of multilevel inverter basically are diode-clasped and capacitor-cinched sort . The previous uses diodes to clasp the voltage level, and the last uses extra capacitors to brace the voltage. The higher number of voltage levels can then be acquired; be that as it may, the circuit turns out to be amazingly intricate in these two topologies. Another sort of multilevel inverter is fell H-Bridge developed by the series association of H-Bridges. The essential circuit is like the traditional H-connect DC–DC converter. The fell structure builds the framework dependability in light of a similar circuit cell, control structure and balance. Be that as it may, the detriments went up against by fell structure are more switches and various data sources. With a specific end goal to build two voltage levels in staircase yield, a H-Bridge developed by four power switches and an individual info are required. Hypothetically, fell H-Bridge can acquire staircase yield with any number of voltage levels, however it is improper to the uses of cost sparing

and info restriction. Various reviews have been performed to build the quantity of voltage levels. An exchanged capacitor (SC) based multilevel circuit can viably expand the quantity of voltage levels. Be that as it may, the control technique is unpredictable, and EMI issue turns out to be more terrible because of the intermittent information current. A solitary stage five-level heartbeat width-adjusted (PWM) inverters constituted by a full scaffold of diodes, two capacitors and switch. In any case, it just gives yield five voltage levels, and higher number of voltage levels is constrained by circuit structure.

A SC-based fell inverter was given Scand full extension backend. In any case, both entangle control and expanded segments constrain its application. The further review was displayed utilizing series/parallel transformation of SC. Be that as it may, it is improper to the applications with HF yield on account of multicarrier PWM (MPWM). In the event that yield frequency is around 20 kHz, the transporter frequency achieves couple of megahertz. In particular, the transporter frequency in MPWMis handfuls times of the yield frequency. Since the bearer frequency decides the exchanging frequency, a high exchanging misfortune is unavoidable for high-frequency yield. A lift multilevel inverter situated in halfway charging of SC can build the quantity of voltage levels hypothetically. In any case, the control methodology is convoluted to actualize fractional charging .Therefore, it is a testing assignment to show a SC-based multilevel inverter with high-frequency yield, low-yield music, and high transformation productivity.

In light of the review circumstance previously mentioned, a novel multilevel inverter and straightforward tweak technique are displayed to fill in as HF power source. Whatever remains of this venture is sorted out as takes after. The dialogs of nine-level inverter are displayed in Section II, including circuit topology, adjustment procedure, operation cycle, and Fourier examination. The parameter assurance and misfortune examination are talked about in Section III. The further improvement of 13-level inverter is examined in Section IV. The execution assessment fulfilled by recreation and analysis is portrayed in Section V.

A. CIRCUIT TOPOLOGY

Fig. 1 shows the circuit topology of nine-level inverter(N1=2,N2=2), whereS1,S2,1,S2as the switching devices of Circuits (SC1 and SC2) are used to convert the series or parallel connection ofC1andC2.S1a,S1b,S1c,S1d,S2a,S2b,S2c,S2dare the switching devices of cascaded H-Bridge.Vdc1 andVdc2are input voltage.D1 andD2 are diodes to restrict the current direction. iout and/or are the output current and the output voltage, respectively.

It is worth noting that the backend circuit of the proposed Inverter is cascaded H-Bridges in series connection. It is significant for H-Bridge to ensure the circuit conducting regardless of the directions of output voltage and current. In other words, Bridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.

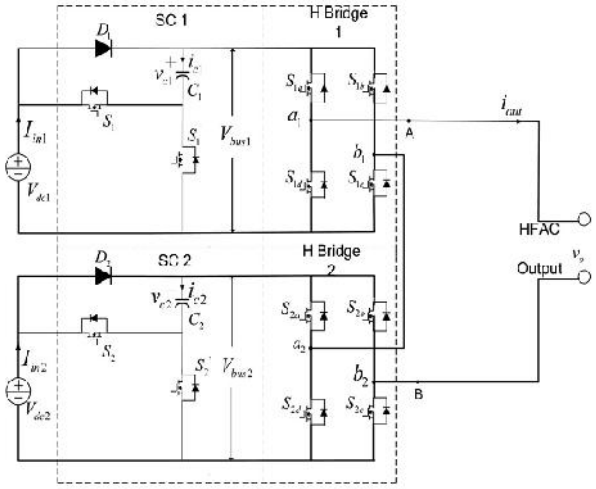


Fig. 1. Circuit topology of cascaded nine-level inverter (N1 =2, N2 =2)

B.SYMMETRICAL MODULATION

There are many modulation methods to regulate the multilevel inverter, the popular modulations are the space vector modulation [22], the multicarrier PWM [23], and the selective harmonic elimination [24], [25], sub harmonic pulse width modulation [26], etc. However, most of them greatly increase the carrier frequency that is dozen times the frequency of reference or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The symmetrical PSMensures the output voltage of full bridge is symmetrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the output frequency [27].

C.OPERATION CYCLES

Fig. 2 demonstrates the ideal waveforms of proposed inverter.Vc are the triangular carrier, and Vpp is the peak value of Vc. The modulation signals of triangular carrier areVm1c, Vm1b, Vm2candVm2b. Vm1b andVm2b are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and is the duration of voltage levels controlled by them. Vm1c andVm2c are used to

control the alternative operations of SC1and SC2, respectively, and is the duration of voltage levels controlled by them.

Thus, the drive signals of H-Bridge switches(S1a,S1b,S1c,S1d,S2a,S2b,S2c,S2d) are phase-shifted pulse signals, while the drive signals of SC switches(S1,S2,S1, S2)are complementary pulse signals. Two operational modes are presented as shown in Fig. 3(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals (Vm1c, Vm1b, Vm2c, and Vm2b). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2. Active circuits of the operational mode 1 are demonstrated in Fig. 4. Re is the equivalent load. When t satisfies t0 ≤t<t1 in Fig. 3(a), the switches S1a, S1b, S2a, S2b are driven byte gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because S1andS2are on, the capacitorsC1 andC2 are charged toxin (Vdc1 =Vdc2 =VIN). The VIN as well.

The current flow of this time interval is shown infix. 3(a). When satisfies t1 ≤t <t2 in Fig. 2(a), the switchesS1a, S1b, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals in. BecauseS1 andS2are on, the capacitorsC1 andC2 keep charged toxin (Vdc1 =Vdc2 =VIN). The voltages on Bus 1 and Bus 2 arriving as well. The current flow of this time interval is shown infix. 3(b). When satisfies t2 ≤t <t3 in Fig. 3(a), the switchesS1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals2Vin. Because S1 andS2are on, the capacitorsC1 andC2 keep charged toxin (Vdc1 =Vdc2 =VIN). The voltages on Bus 1 and Bus 2 arriving as well. The current flow of this time interval is shown in Fig. 3(c).

When satisfies t3 ≤t <t4 in Fig. 2(a), the switches S1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 3Vin. BecauseS1andS2are on, the capacitorC1keeps charged toxin (Vdc1 =Vdc2 =VIN), and the capacitorC2is discharged. The voltages on Bus 1 and Bus 2 arriving and 2Vin, respectively. The current flow of this time interval is shown infix. 3(d)

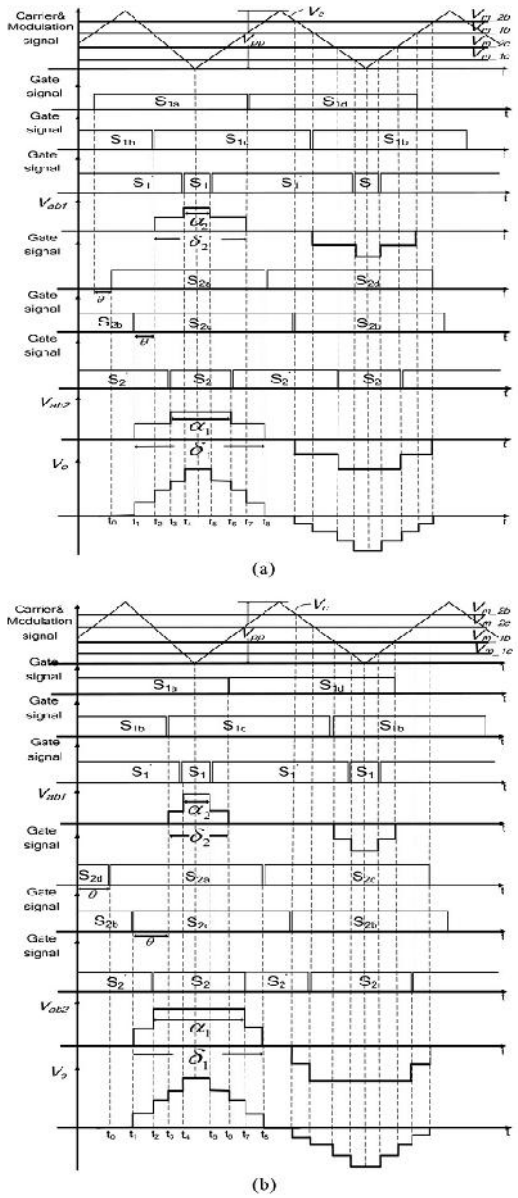


Fig. 2. Operational waveforms of the proposed multilevel inverter. (a) Operational mode 1. (b) Operational mode 2.

When satisfies t4 ≤t <t5 in Fig. 3(a), the switchesS1a, S1c, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals 4Vin. Because S1 andS2 are on, the capacitorC1 andC2 are discharged. The voltages on Bus 1 and Bus 2both are 2Vin. The current flow of this time interval is shown in Fig. 3(e).

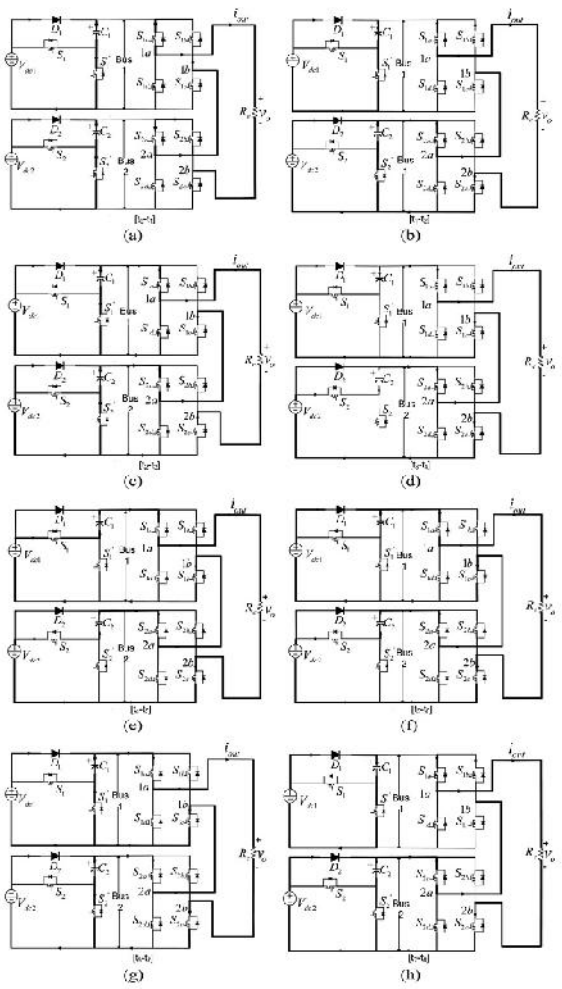


Fig. 3. Active circuits for different operation intervals in the operational mode
1: (a)t0−t1;(b)t1−t2;(c)t2−t3;(d)t3−t4;(e)t4−t5; (f) t5−t6; (g)t6−t7;(h)t7−t8.

The operations int5≤t<t6, t6≤t<t7, andt7≤t<t8, are the same as the operations int3≤t<t4, t2≤t<t3, andt1≤t<t2, respectively. The active circuits are shown in Fig. 4(f)–(h).Comparing with operational mode 1, the mode 2 has the different active circuits in two time intervals. Whentsatisfiest2≤t<t3in operational mode 2 as shown in Fig. 3(b), the switchesS1a, S1b, S2a, S2c are driven by the gate-source voltage, respectively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in

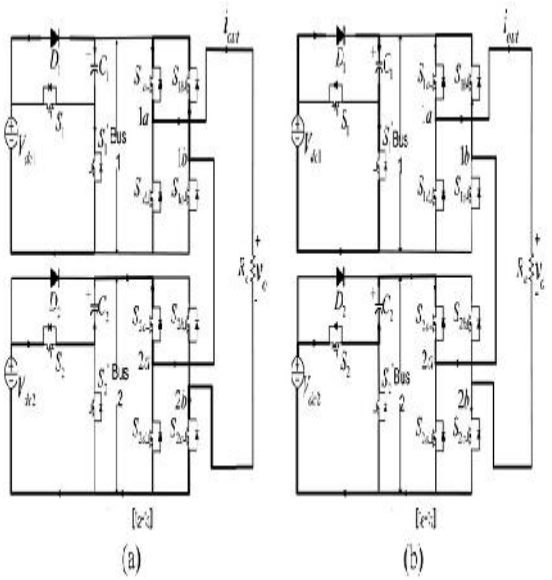


Fig. 4. Active circuits for different operation intervals in the operational mode 2: (a) t2−t3 ;(b) t6−t7.

Positive conducting state. Output voltage equals 2Vin. Because1 andS2 are on, the capacitorC1 keeps charged toxin andcapacitorC2is discharged. The voltages on Bus 1 and Bus 2 arriving and 2Vin, respectively. The current flow of this time intervals shown in Fig. 5(a). Similarly, the active circuit of t6≤t<t7is shown in Fig. 5(b) that has the same operations as t2 ≤t <t3.

The second half-cycle (fromt8 on) has the similar active circuits as the first half-cycle (t1−t8), but the current will be circulated in the opposite direction to provide the negative output voltage. The relations of on-state switches and output voltage level are described in Table I, as well as operations of two modes am compared closely. Table I hasten working states for nine voltage levels. When the operation enters a new state from an adjacent state, only one power switch changes between on and off. The device stress in switching devices of H-bridge circuit is higher than that in SC circuit. It can also be found that the output voltage in Mode 1 is more stable than Mode 2 due toeless discharging period of switching capacitor.

Along with the up-down movement of modulation signals (Vm1c, Vm1b, Vm2c, Vm2b), the output voltage of the proposed inverter is a controllable nine-level staircase. The duration of each voltage level is determined by the duty-cycle of Circuit and the phase-shifted angle of H-Bridge circuit. Operating cycles of the proposed topology explained in(1)

TABLE I
RELATIONS OF ON-STATE SWITCHES AND OUTPUT VOLTAGE

Mode 1			Mode 2		
On-state switches	Output voltage	Capacitor State	On-state switches	Output voltage	Capacitor State
$S_{11}, S_{12}, S_{21}, S_{22}, S_1, S_2'$	$4V_{dc}$	C_1, C_2 Discharging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1, S_2'$	$4V_{dc}$	C_1, C_2 Discharging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2$	$3V_{dc}$	C_2 Discharging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2$	$3V_{dc}$	C_2 Discharging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$2V_{dc}$	C_1, C_2 Charging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$2V_{dc}$	C_2 Discharging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	V_{dc}	C_1, C_2 Charging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	V_{dc}	C_1, C_2 Charging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$ or $S_{11}, S_{12}, S_{21}, S_{22}$	0	C_1, C_2 Charging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$ or $S_{11}, S_{12}, S_{21}, S_{22}$	0	C_1, C_2 Charging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-V_{dc}$	C_1, C_2 Charging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-V_{dc}$	C_1, C_2 Charging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-2V_{dc}$	C_1, C_2 Charging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-2V_{dc}$	C_2 Discharging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-3V_{dc}$	C_2 Discharging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1', S_2'$	$-3V_{dc}$	C_2 Discharging
$S_{11}, S_{12}, S_{21}, S_{22}, S_1, S_2'$	$-4V_{dc}$	C_1, C_2 Discharging	$S_{11}, S_{12}, S_{21}, S_{22}, S_1, S_2'$	$-4V_{dc}$	C_1, C_2 Discharging

It can be found that THD is easy to be regulated byte duration width of voltage levels. At the suitable scope ofx1andx2, THD of output voltage is less than 10%. Whenk1=0.6andk2=0.4, THD can be less than 10% within the scope of 0.05<x1<0.5 and0.4<x2<0.6. Whenk1=0.5 andk2=0.5, THD can be less than 10% within the scope of 0<x1<0.4 and0.4<x2 <0.6. Furthermore, THD becomes less along with the increasing number of voltage levels. The output magnitude of multilevel inverter can be regulated by the duration width of voltage levels as well. Two patterns are available to perform the regulations of THD and magnitude simultaneously. One is toregulatex1, x2with the fixedk1, K2. The other one is to regulatek1, k2with the fixedx1, x2. The numerical benchmark and THD optimization will be examined in the future study, and a fixed ratio (k1 =K2=0.5, x1=π/8, x2=π/4) is adopted to evaluate output harmonics in subsequent simulation and experiment. If the proposed dc–ac inverter is used as second stage oaf–ac conversion, an ac–dc controlled rectifier is introduced as preceding stage of ac–ac conversion. Power factor correction (PFC) implemented by dc–dc converter can improve the power factor in ac–dc conversion. In this case, both SC and H-bridge generate the optimized pulse width to minimize output THD. The magnitude regulation of output voltage can be performed by controllable ac–dc stage in input side. The minimized this achieved by this two-stage power circuit, namely, ac–dc stages used to regulate magnitude, and dc–ac stage formed by the proposed inverter is used to minimize THD.

D. Simulation Evaluation

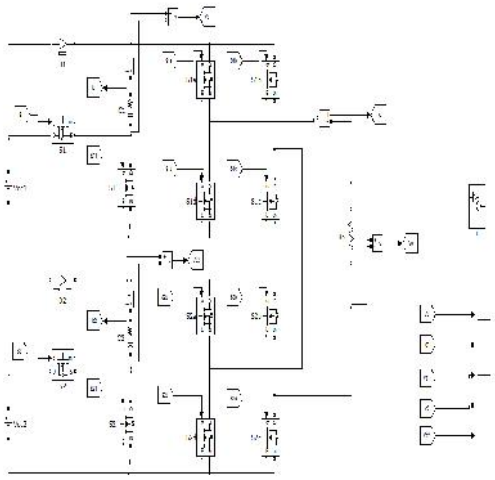


Fig5:Simulation block diagram of 9-level inverter

The simulation based on PSIM is performed for the proposed inverter. The waveforms of output voltage vow, capacitor currents (iC1, iC2) and capacitor voltages (vC1, vC2) are shown infix. 10. The following parameters are used for low power simulation. The input voltage Irvin =12 V, the module 1 capacitorisC1=100μF with 80 mesh, the module 2 capacitor isC2=220μF with 50 mesh, the diodesD1 andD2 have 0.6 Forward voltage drop and 50 mΩ internal on-state resistance, and the load resistance sire=12Ω.

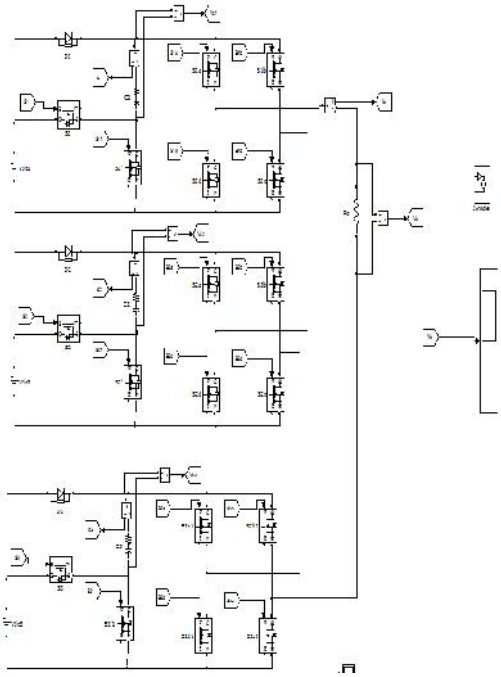


Fig6:Simulation block diagram of 13-level inverter

ISSN 2321-6905
January -2017

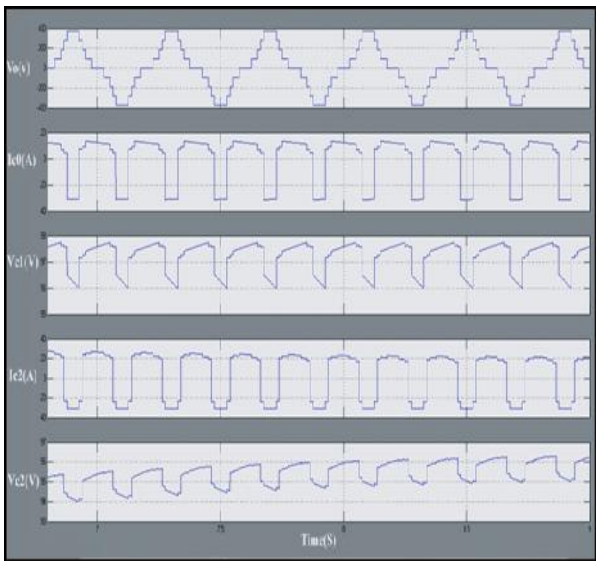
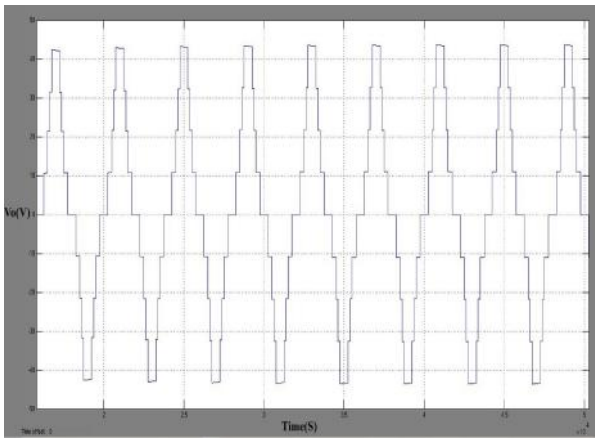
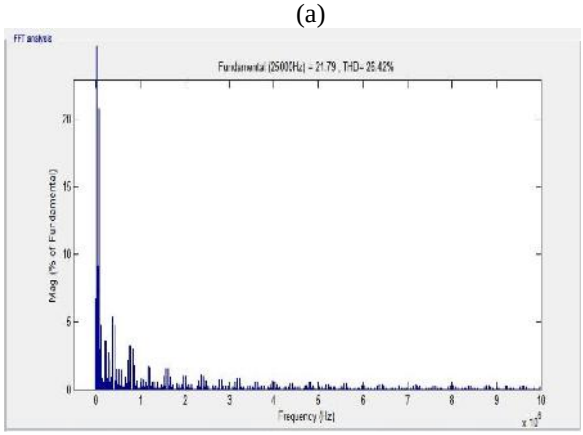


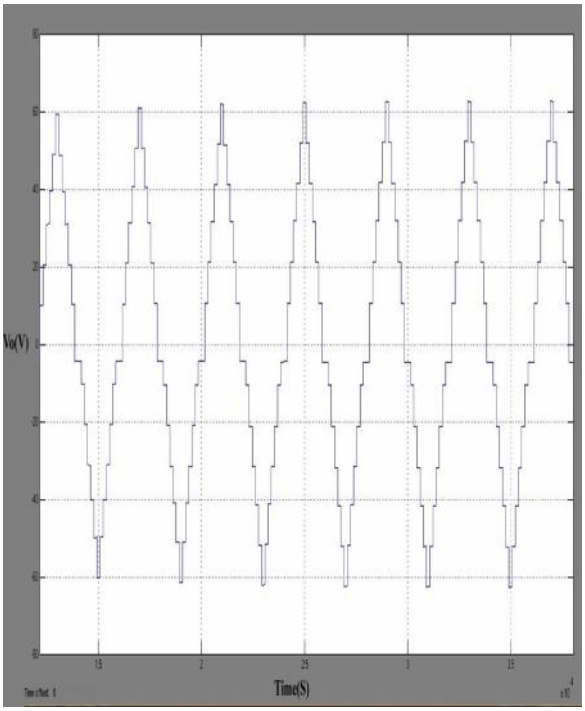
Fig. 7. Simulation waveforms of nine-level SC-based cascaded inverter, output frequency's =25 kHz (k1 =K2 =0.5, x1 =π/8, x2 =π/4, High power at 4 kW



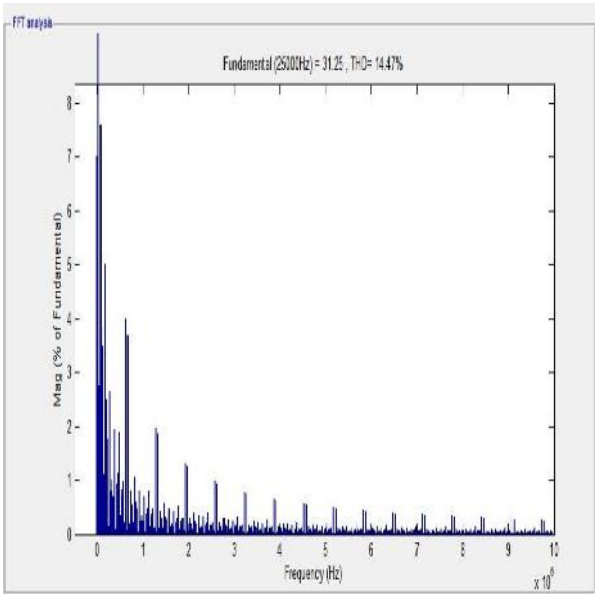
(a)



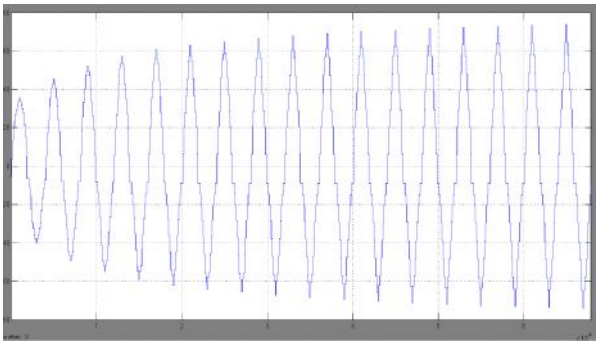
(b)



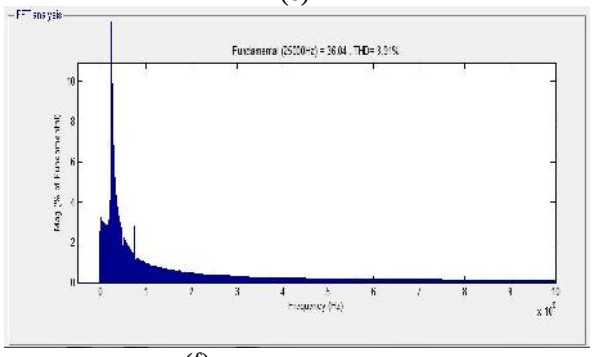
(c)



(d)



(e)



(f)

Fig. 8. Simulation waveforms of 9-level and 13-level inverter, output frequency's =25 kHz. (a) Output voltage of nine-level inverter (k1 =K2 =0.5, x1 =π/8, x2 =π/4). (b) Spectrum of nine-level output. (c) Output voltage of13-level inverter (same duration of each voltage level). (d) Spectrum of 13-level output.(e) 17-level inverter output
(f)THD of 17 level

CONCLUSION

In this project, a novel SC-based cascaded multilevel inverter was proposed. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded multilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method. Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases twice in half cycle of 9-level circuit, and the number of voltage levels increases three times in half cycle of 13-level circuit. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology and total harmonic distortion is reduced in 17 and 13- level inverter when compared to 9-level inverter the Meanwhile, the magnitude control can be accomplished by pulse width regulation of voltage level, so the proposed multilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This project mainly analyzes nine-level ,13 and 17-level inverters. The method of analysis and design is also applicable to other members of the proposed inverter. The proposed inverter can be applied to grid-connected photovoltaic system and electrical network of EV, because the multiple dc sources are available easily from solar panel, batteries, ultra capacitors, and fuel cells.

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