



## Design And Implementation of Modular Multilevel Inverter With Reduced Number Of Components

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### ABSTRACT-

In this paper, utilizing H-connect topology a general course multilevel inverter for the execution of 49th level inverter and another calculation in producing all voltage levels for a 49th level with less number of dc sources. Brings about diminished intricacy and practical. The examination is finished with the customary topologies and affirmed by recreation comes about.

*Index Terms*— voltage source inverter, developed H-bridge, multilevel inverter, Cascaded multilevel inverter.

### I. INTRODUCTION

With the advancement in inverters, multilevel inverters have received more attention because high-power and medium voltage ratings provides advantage in of high power quality, lower order harmonics, and better electromagnetic interference etc. By appropriately arranging the semi-conductor based switches the inverter will generate a stepped voltage waveform. The primary structures of the multilevel inverters have been exhibited: "diode clasped multilevel inverter", "flying capacitor multilevel inverter," and "fell multilevel inverter". Multilevel inverters is made out of symmetric and deviated bunches in view of the dc voltage sources.

The fell multilevel inverter is made out of various single-stage H-connect inverters and is arranged into symmetric and hilter kilter bunches in view of the extent of dc voltage sources. In the symmetric sorts, the sizes of the dc voltage wellsprings of all H-extensions are equivalent while in the awry sorts, the estimations of the dc voltage wellsprings of all H-scaffolds are distinctive. As of late, a few topologies with different control methods have been introduced for fell multilevel inverters [5]–[8]. In [4] and [9]–[15], distinctive symmetric fell multilevel inverters have been exhibited. The primary preferred standpoint of

every one of these structures is the low assortment of dc voltage sources, which is a standout amongst the most imperative components in deciding the cost of the inverter. Then again, on the grounds that some of them utilize a high number of bidirectional power switches, a high number of protected entryway bipolar transistors (IGBTs) are required, which is the primary hindrance of these topologies. A lopsided topology has been exhibited in [16]. The primary inconvenience of this structure is identified with its bidirectional power switches, which cause an expansion in the quantity of IGBTs and the aggregate cost of the inverter. In [15], another topology with three calculations have been exhibited, which decrease the quantity of required power switches yet increment the assortment of dc voltage sources. In [1], [4] and [17], and [18], a few calculations for deciding the extents of dc voltage hotspots for the customary fell multilevel inverter have been exhibited. The significant preferred standpoint of this topology and its calculations is identified with its capacity to produce an impressive number of yield voltage levels by utilizing a low number of dc voltage sources and power switches yet the high assortment in the extent of dc voltage sources is their most wonderful weakness. In this paper, with a specific end goal to expand the quantity of yield voltage levels and diminish the quantity of energy switches, driver circuits, and the aggregate cost of the inverter, another topology of fell multilevel inverters is proposed. It is critical to note that in the proposed topology, the unidirectional power switches are utilized. At that point, to decide the size of the dc voltage sources, another calculation is proposed. Also, the proposed topology is contrasted and different topologies from various perspectives, for example, the quantity of IGBTs, number of dc voltage sources, the assortment of the estimations of the dc voltage sources, and the estimation of the blocking voltages per switch. At long last, the execution of the proposed topology in creating all voltage levels through a 49 - level inverter is affirmed by MATLAB reenactment.

### II. PROPOSED TOPOLOGY

In Fig. 1, two new topologies are proposed for a seven-level inverter [19]. As appeared in Fig. 1, the proposed topologies are gotten by including two unidirectional power switches and one dc voltage source to the H-connect inverter structure. At the end of the day, the proposed inverters are included six unidirectional power switches ( $S_a, S_b, S_{L,1}, S_{L,2}, S_{R,1},$  and  $S_{R,2}$ ) and two dc voltage sources ( $V_{L,1}$  and  $V_{R,1}$ ). In this paper, these topologies are called developed H-bridge. As shown in Fig. 1, the simultaneous turn-on of  $S_{L,1}$  and  $S_{L,2}$  (or  $S_{R,1}$  and  $S_{R,2}$ )

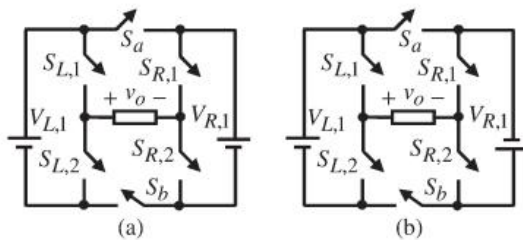


Fig. 1. Proposed seven-level inverters. (a) First proposed topology. (b) Second proposed topology.

No	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	$S_a$	$S_b$	Inverters (a) First proposed topology	Inverters (b) First proposed topology
1	1	0	0	1	0	1	$V_{L,1} - V_{R,1}$	$V_{L,1} - V_{R,1}$
2	1	0	0	1	1	0	$V_{L,1} - V_{R,1} - V_{L,2}$	$V_{L,1} - V_{R,1} - V_{L,2}$
3	1	0	1	0	0	1	$V_{L,1} - V_{R,1} + V_{R,2}$	$V_{L,1} - V_{R,1} + V_{R,2}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1} - V_{R,1} - V_{L,2}$	$-V_{L,1} - V_{R,1} - V_{L,2}$
6	0	1	1	0	0	1	$-V_{L,1} - V_{R,1} + V_{R,2}$	$-V_{L,1} - V_{R,1} + V_{R,2}$
7	0	1	0	1	1	0	$-V_{L,1} - V_{R,1} - V_{L,2}$	$-V_{L,1} - V_{R,1} - V_{L,2}$

causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition,  $S_a$  and  $S_b$  should not turn on, simultaneously. The distinction in the topologies delineated in Fig. 1 is in the association of the dc voltage sources extremity. Table I demonstrates the yield voltages of the proposed inverters for various conditions of the switches. In this table, 1 and 0 show the ON-and OFF-conditions of the switches, individually. As it is evident from Table I, if the estimations of the dc voltage sources are equivalent, the quantity of voltage levels abatements to three. Along these lines, the estimations of dc voltage sources ought to be distinctive to create more voltage levels without expanding the quantity of switches and dc voltage sources. Considering Table I, to produce all voltage

levels (odd and even) in the proposed topology appeared in Fig. 1(a), the extents of  $V_{-(L,1)}$  and  $V_{-(R,1)}$  ought to be viewed as 3pu and 1pu, separately. Thus, for the topology appeared in Fig. 1(a), the extents of  $V_{-(L,1)}$  and  $V_{-(R,1)}$  ought to be viewed as 2pu and 1pu, individually. Considering the previously mentioned clarifications, the aggregate cost of the proposed topology in Fig. 1(b) is low since dc voltage sources with low sizes are required. By building up the seven-level inverter appeared in Fig. 1(b), the 31-level inverter appeared in Fig. 2 can be proposed. This topology comprises of ten unidirectional power switches and four dc voltage sources. As per Fig. 2, if the power switches of ( $S_{-(L,1)}, S_{-(L,2)}$ ), ( $S_{-(L,3)}, S_{-(L,4)}$ ), ( $S_{-(R,1)}, S_{-(R,2)}$ ), and ( $S_{-(R,3)}, S_{-(R,4)}$ ) turn on all the while, the dc voltage sources of  $V_{-(L,1)}, V_{-(L,2)}, V_{-(R,1)}$ , and  $V_{-(R,2)}$  will be shortcircuited, individually. Consequently, the concurrent turn-on of these switches ought to be kept away from. In addition,  $S_a$  and  $S_b$  should not turn on simultaneously. It is important to note that the 127-level topology can be provided through the structure presented in Fig. 1(a), where the only difference will be in the polarity of the applied dc voltage sources. By developing the proposed 49<sup>th</sup> level inverter, a 49<sup>th</sup> -level inverter can be proposed as shown in Fig. 3. This topology

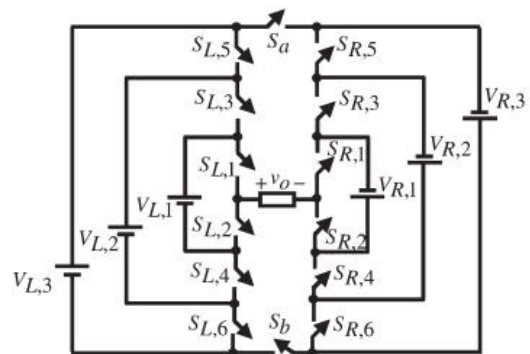


Fig. 3. Proposed 49-level inverter.

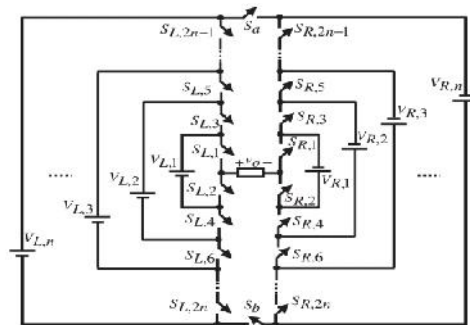


Fig. 4. Proposed general topology.

consists of 14 unidirectional power switches and 6 dc voltage sources. Similarly, by developing the proposed basic topology, a general topology, as shown in Fig. 4, can be proposed. The general topology consists of  $2n$  dc voltage sources ( $n$  is the number of the dc voltage sources on each leg) and  $4n + 2$  unidirectional power switches. In the proposed general topology, the number of output voltage levels ( $N_{step}$ ), number of switches ( $N_{switch}$ ), number of dc voltage sources ( $N_{source}$ ), and the maximum magnitude of the generated voltage ( $V_{o,max}$ ) are calculated as follows, respectively:

$$N_{step} = 2^{2n+1} - 1 \quad \text{----- (1)}$$

$$N_{switch} = 4n + 2 \quad \text{----- (2)}$$

$$N_{source} = 2n \quad \text{----- (3)}$$

$$V_{o,max} = V_{L,n} + V_{R,n} \quad \text{----- (4)}$$

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [20]. The number of variety of the values of dc voltage sources ( $N_{variety}$ ) is given by

$$N_{variety} = 2n \quad \text{----- (5)}$$

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig. 1(b), the blocking voltage of  $S_{R,1}$  and  $S_{R,2}$  are calculated as follows:

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad \text{----- (6)}$$

Where  $V_{SR,1}$  and  $V_{SR,2}$  indicate the maximum blocking voltages of  $S_{R,1}$  and  $S_{R,2}$ , respectively. The blocking voltage of  $S_{L,1}$  and  $S_{L,2}$  are as follows:

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad \text{----- (7)}$$

Where  $V_{SL,1}$  and  $V_{SL,2}$  indicate the maximum blocking voltages of  $S_{L,1}$  and  $S_{L,2}$ , respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter ( $V_{block,1}$ ) is calculated as follows:

$$\begin{aligned} V_{block,1} &= V_{SR,1} + V_{SR,2} + V_{SL,1} + V_{SL,2} + V_{Sa} + V_{Sa} \\ &= 4(V_{R,1} + V_{L,1}) \end{aligned} \quad \text{----- (8)}$$

Considering Fig. 2, the maximum blocking voltage of the switches is as follows:

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad \text{----- (9)}$$

$$V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \quad \text{----- (10)}$$

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad \text{----- (11)}$$

$$V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \quad \text{----- (12)}$$

$$V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2} \quad \text{----- (13)}$$

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter ( $V_{block,2}$ ) is as follows:

$$\begin{aligned} V_{block,2} &= V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} \\ &\quad + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} \\ &= 4(V_{R,2} + V_{L,2}) \end{aligned} \quad \text{----- (14)}$$

Similarly, the maximum blocking voltage of all switches of the 49-level inverter is calculated as follows:

$$V_{block,3} = 4(V_{R,3} + V_{L,3}) \quad \text{----- (15)}$$

Finally, the maximum blocking voltage of all the switches of the general topology ( $V_{block,n}$ ) is calculated as follows:

$$V_{block,n} = 4(V_{R,n} + V_{L,n}) \quad \text{----- (16)}$$

### III. PROPOSED ALGORITHM TO DETERMINE THE MAGNITUDES OF DC VOLTAGE SOURCES

In this paper, the following algorithm is applied to determine the magnitude of dc voltage sources. It is important to note that all voltage levels (even and odd) can be generated.

#### A. Proposed 49-Level Inverter

The magnitudes of the dc voltage sources of the proposed 127-level inverter are calculated as follows:

$$V_{L,1} = V_{dc} \quad \text{----- (17)}$$

$$V_{R,1} = 2V_{dc} \quad \text{----- (18)}$$

$$V_{L,2} = 5V_{dc} \quad \text{----- (19)}$$

$$V_{R,2} = 10V_{dc} \quad \text{----- (20)}$$

$$V_{L,3} = 25V_{dc} \quad \text{----- (21)}$$

$$V_{R,3} = 50V_{dc} \quad \text{----- (22)}$$

By using this algorithm, the inverter can generate all negative and positive voltage levels from 0 to  $63 V_{dc}$  with steps of  $V_{dc}$

#### D. Proposed General Multilevel Inverter

The magnitudes of the dc voltage sources of the proposed general multilevel inverter can be obtained as follows:

$$V_{Lj} = 5^{j-1}V_{dc} \text{ for } j = 1, 2, 3, \dots, n \quad (23)$$

$$V_{Rj} = 2 \times 5^{j-1}V_{dc} \text{ for } j = 1, 2, 3, \dots, n \quad (24)$$

Considering (4) and (16), the values of  $V_{o,max}$  and  $V_{block,n}$  of the proposed general multilevel inverter are as follows, respectively:

$$V_{o,max} = V_{L,n} + V_{R,n} = 3 \times 5^{n-1}V_{dc} \quad (25)$$

$$V_{block,n} = 4(V_{L,n} + V_{R,n}) = 12(5^{n-1})V_{dc} \quad (26)$$

#### IV. CALCULATION OF LOSSES

Mainly, two kinds of losses (i.e., conduction and switching losses) are associated with the switches. Since the switches include IGBTs and diodes, the conduction losses of an IGBT ( $p_{c,IGBT}(t)$ ) and a diode ( $p_{c,D}(t)$ ) are calculated as follows, respectively [7], [22]:

$$p_{c,IGBT}(t) = [V_{IGBT} + R_{IGBT}i^\beta(t)]i(t) \quad (27)$$

$$p_{c,D}(t) = [V_{IGBT} + R_{IGBT}i^\beta(t)]i(t) \quad (28)$$

Where  $V_{IGBT}$  and  $V_D$  are the forward voltage drops of the IGBT and diode, respectively.  $R_{IGBT}$  and  $R_D$  are the equivalent resistances of the IGBT and diode, respectively, and  $\beta$  is a constant related to the specification of the IGBT. Considering that at instant  $t$ , there are  $N_{IGBT}$  transistors and  $N_D$  diodes in the current path, the average value of the conduction power loss ( $P_c$ ) of the multilevel inverter can be written as follows:

$$P_c = \frac{1}{2} \int_0^{2\pi} [N_{IGBT}(t)p_{c,T}(t) + N_D(t)p_{c,D}(t)] dt \quad (29)$$

The switching losses are calculated based on the energy loss calculation. The switching losses occur during the turn-off and turn-on periods. For simplicity, the linear variations of the voltage and current of the switches in the switching period are considered. Based on this assumption, the following relations can be written [7], [22]:

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}It_{off} \quad (28)$$

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}I't_{on} \quad (29)$$

Where  $E_{off,k}$  and  $E_{on,k}$  are the turn-off and turn-on losses of the switch  $k$ , respectively.  $t_{off}$  and  $t_{on}$  are the turn-off and turn-on times of the switch, respectively,  $I$  is the current through the switch before turning off,  $I'$  is the current through the switch after turning on, and  $V_{sw,k}$  is the OFF-state voltage on the switch. The switching power loss ( $P_{sw}$ ) is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage. This can be written as follows [7], [22]:

$$P_{sw} = f \sum_{k=1}^{N_{switch}} \left( \sum_{i=1}^{N_{on,k}} E_{on,k,i} + \sum_{i=1}^{N_{off,k}} E_{off,k,i} \right) \quad (30)$$

Where  $f$  is the fundamental frequency and  $N_{on,k}$  and  $N_{off,k}$  are the numbers of turn-on and turn-off of the switch  $k$  during a fundamental cycle. Also,  $E_{on,ki}$  is the energy loss of the switch  $k$  during the  $i$ th turn-on and  $E_{off,ki}$  is the energy loss of the switch  $k$  during the  $i$ th turn-off. The total loss ( $P_{loss}$ ) of the multilevel converter is the sum of the conduction and switching losses as follows:

$$P_{loss} = P_c + P_{sw} \quad (31)$$

Finally, the efficiency ( $\eta$ ) of the inverter is calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (32)$$

Where  $P_{out}$  and  $P_{in}$  denote the output and input powers of the inverter.

#### V. COMPARING THE PROPOSED GENERAL TOPOLOGY WITH THE CONVENTIONAL TOPOLOGIES

In order to clarify the advantages and disadvantage of the proposed topology, it should be compared with the different kinds of topologies presented in literature. In [4], the conventional cascaded multilevel inverter with two different algorithms has been presented. These algorithms are known as the symmetric cascaded multilevel inverters and the asymmetric ones with the binary method for determining the magnitude of dc voltage sources. In the comparison, the conventional symmetric cascaded multilevel inverter is indicated by

$R_1$  and the conventional binary asymmetric cascaded multilevel inverter is shown by  $R_2$ . Three other algorithms have been presented for this topology in [1], [17], and [18], which are indicated by  $R_3$ – $R_5$ , respectively. Moreover, another topology with three different algorithms for determining the value of dc voltage sources has been introduced in [15], which are shown by  $R_{13}$ – $R_{15}$  in this comparison. In [9]–[12], four different structures for the cascaded multilevel inverter have been presented, and in this paper, they are indicated by  $R_6$ – $R_7$  and  $R_{11}$ – $R_{12}$ . It is important to note that the power switches in the aforementioned topologies are unidirectional. In addition, other topologies based on bidirectional switches have been presented in [13] and [14]. In [14], three different algorithms have been recommended, which are denoted as  $R_8$ – $R_{10}$ , and the presented topology in [13] is indicated by  $R_{16}$  in this comparison. Fig. 5 shows all of the aforementioned structures. Fig. 6 compares the number of IGBTs of the proposed general topology with the aforementioned cascaded multilevel inverters. It is obvious that the proposed inverter requires a lesser number of IGBTs in comparison with the other mentioned topologies to generate particular levels. Fig. 7 compares the number of dc voltage sources of the proposed inverter with the aforementioned cascaded multilevel inverter. As shown in Fig. 7, the proposed inverter has better performance in comparison with the other presented topologies except the topology presented in  $R_3$ . However, the magnitude of the dc voltage sources in  $R_3$  is a little more than that of the proposed topology.

Fig. 8 compares the variety of magnitudes of the dc voltage sources of the proposed inverter with that of the aforementioned cascaded multilevel inverter. Obviously, the proposed inverter uses a wider variety of magnitudes of the dc voltage sources in comparison with those of all the aforementioned topologies. This feature is the most important disadvantage of the proposed topology because the variety of the values of dc voltage sources is as one of the remarkable factors in determining the cost of the inverter. However, this feature in the proposed topology is similar to the presented topologies of  $R_2$

and  $R_{14}$ . Fig. 9 compares the magnitude of the blocking voltage of the switches of the proposed inverter with that of the aforementioned cascaded multilevel inverter. This figure shows the reduction of the magnitude of the blocking voltage of the proposed inverter in comparison with those of all the aforementioned multilevel inverters.

## VI. SIMULATION RESULTS

In order to verify the correct performance of the proposed multilevel inverter in generating all output voltage levels (even and odd), a 49-level inverter based on the topology shown in Fig. 2 has been used for the simulation. Table II shows the switching states of the 49-level inverter.

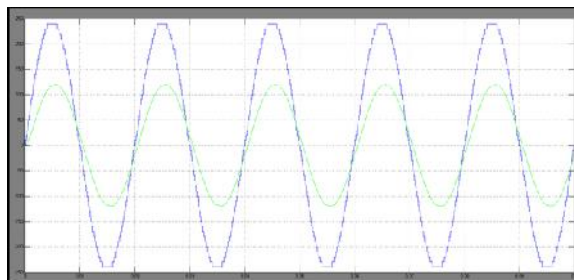
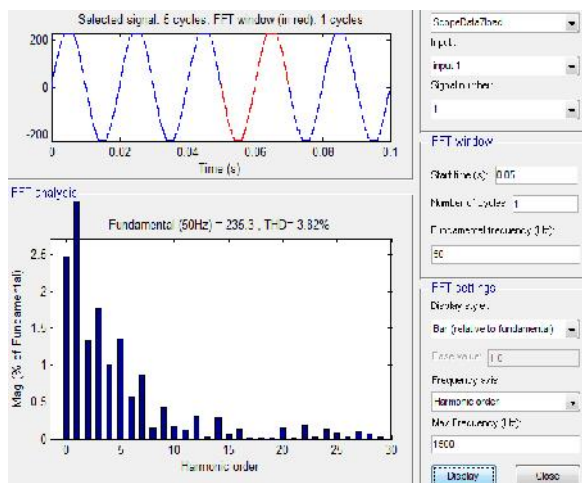


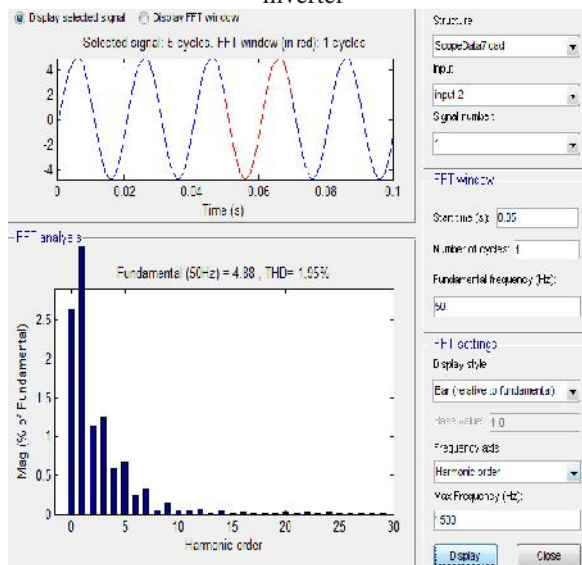
Fig. 11 49 level voltage and current

The simulation is done by using MATLAB software, and the practical prototype is made in the experimental environment. Fig. 10 shows the experimental setup. It is important to note that the IGBTs used in the prototype are HGTP10N40CID (with an internal anti-parallel diode) with the voltage and current ranges of 400 V and 10 A, respectively. The 89C52 microcontroller by ATMEL Company has been used to generate all switching patterns. In all processes of the simulation and experiment, the load is assumed as R–L with  $R=45$  and  $L=55$ mH. Moreover, the magnitude of  $V_{L,1}$  is considered 15 V, so based on (29) and (30), the magnitudes of the other dc voltage sources will be 30, 75, and 150 V, which are related to  $V_{R,1}$ ,  $V_{L,2}$ , and  $V_{R,2}$ , respectively. According to (31), the maximum output voltage of this inverter will be 225 V. In this paper, the fundamental frequency switching control method has been used [21]. In this method, the sinusoidal reference voltage is compared with the available dc voltage levels and the level that is nearest to the reference voltage is chosen [22]. The main advantage of this control method is related to its low switching frequency, which leads to reduction of switching losses. The simulated output voltage and current waveforms are shown in Fig. 11. As Fig. 11(a) shows, the proposed topology is able to generate 31 levels (15 positive levels, 15 negative levels, and 1 zero level) with the maximum voltage of 225 V. Comparing the output voltage and current waveforms indicates that the output current waveform is more similar to the ideal sinusoidal waveform than the output voltage because the R–L load acts as a low-pass filter. In addition, there is a phase difference between the output voltage and current waveforms, which is caused by the inductive feature of the load. The total harmonic distortions of the output voltage and current are equal to 0.94% and 0.19%, respectively. Fig. 12(a) and (b) shows the

harmonic spectrum of the output voltage and current, respectively. The figure shows that the magnitudes of harmonics of both voltage and current waveforms are low. However, the harmonics of the current waveform are lower than the voltage



(a) Harmonic spectrum of output voltage of 31 level inverter



(b)

Fig. 12. Harmonic spectrum of (a) output voltage of 49 level inverter

considered nonlinear. In the test condition, the measured input and output powers are about 1203 and 1112 W, respectively. Therefore, the efficiency is about 92.4%. Based on the loss calculations given before, the power loss is about 86 W. Therefore, the calculated loss has a good accordance with the measured efficiency. As mentioned before, the power switches in the proposed topology are unidirectional from the voltage viewpoint.

In order to prove this issue, the voltages on the switches of a single leg of the inverter (*i.e.*,  $S_{L,1}$ ,  $S_{L,2}$ ,  $S_{L,3}$ ,  $S_{L,4}$ , and  $S_a$ ) are shown in Fig. 13. As can be seen, the maximum blocking voltage by switches  $S_{L,1}$ ,  $S_{L,2}$ ,  $S_{L,3}$ ,  $S_{L,4}$ , and  $S_a$  are equal to 15, 15, 60, 60, and 225 V, respectively. Obviously, the voltage values are zero or equal to the positive ones, which is well in accordance to the unidirectional feature of the switches from the voltage view point. Considering the magnitude of the blocking voltage of the switches, the relations associated to the maximum voltage drop of the switches are well confirmed. Fig. 14 shows the experimental results of the implemented inverter. It is important to note that there is a good agreement between the experimental and simulation results.

### VII. CONCLUSION

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 49-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower

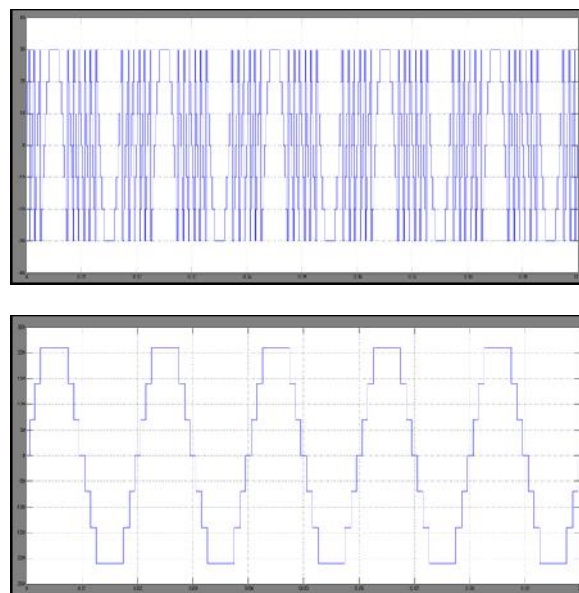


Fig. 13. Voltages of switches (a)  $S_{L,1}$ , (b)  $S_{L,2}$

than that of conventional topologies. However, the proposed topology has a higher number of variety of dc

voltage sources in comparison with the others. The performance accuracy of the proposed topology was verified through the MATLAB simulation and the experimental results of a 49-level inverter.

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