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7 Level Hybrid Neutral Point Flying Capacitor Multilevel Inverter

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Abstract-

This work proposes another seven-level hybrid topology joining components of neutral point braced and flying capacitor inverters. The proposed topology gives a tradeoff between various part checks to accomplish a decent loss dissemination, evade coordinate arrangement association of semiconductor gadgets, keep the adjusted operation of dc-connection capacitors while keeping the quantity of expensive segments, for example, capacitors and switches low. The required balance methodology is created and the operation of the proposed topology is contemplated. The elements of the proposed topology are examined and contrasted with other accessible topologies. Reenactment results are given to check the execution of the converter for medium voltage applications. Recreation comes about check through MATLAB/SIMULINK condition.

Key words- flying capacitor, Neutral point, Matlab.

INTRODUCTION

Multilevel inverters have picked up enthusiasm amid the most recent three decades because of the expanding interest for medium to high voltage converters for an assortment of high power applications. Diverse topologies have been proposed to fit the prerequisites of various applications. For medium voltage inverters, Cascade H-connect (CHB), impartial point clipped (NPC), and flying capacitor (FC) are the essential topologies. Among them, NPC and FC give a typical dc-interface which is a strict prerequisite for some applications. FC inverter utilizes capacitors to create yield voltage levels. The accessibility of intra-phrasal excess states in this topology can give both capacitor voltage adjusting and control misfortune circulation among switch. Be that as it may, expanded number of flying capacitors at larger amounts that builds the underlying expense and support extra charges and reductions the dependability of the inverter alongside the capacitor pre charge in a few applications are the principle disadvantages of this topology.

NPC inverter utilizes diodes to brace the voltage levels produced at the dc-interface capacitors to the yield. Inordinate number of diodes, lopsided operation of dc-connection's voltage divider capacitors, and uneven dissemination of misfortune among switches are significant issues of this topology. Space vector calculations are accessible to ease the uneven misfortune and capacitor voltage issues in view of the inverter's working condition. Dynamic NPC (ANPC) enhances the misfortune appropriation of NPC by supplanting diodes with dynamic switches giving option unbiased point way.

Half and half topologies are suitable arrangements where higher number of levels is required. Joining the benefits of CHB, FC, and NPC, half breed inverters can give misfortune and voltage adjusting while at the same time keeping the quantity of segments low. Cases of half and half topologies joining FC and NPC can be found in , some of which has effectively discovered mechanical applications. The 5-level FC-ANPC is a case of cross breed topologies that advanced toward the business. The ACS2000 group of medium voltage drives, popularized by ABB, utilizes this topology with both dynamic and uninvolved front end arrangements. The primary preferred standpoint of this topology is the utilization of a solitary flying capacitor to create the yield five levels. Contrasted with different topologies that give a typical dc-connect, FC-ANPC has given an adequate tradeoff between the cost, execution, and dependability for 5-level applications. The burdens of FC-ANPC are high number of switches, arrangement association of high voltage switches, and poor misfortune conveyance.

This venture proposes another 7-level crossover topology in view of FC and NPC inverters. The objective of the proposed topology is to defeat the weaknesses of the conventional FC-ANPC. In this way, similarly, the proposed topology gives better misfortune dispersion, stays away from direct arrangement association of high voltage switches, and wipes out 2 switches per stage leg. These points of interest come at the cost of an extra capacitor and 6 diodes. In any case, the lifetime of every capacitor is relied upon to delay because of the half cycle operation and lower rms current.

In this venture, the design and operation of the proposed topology is portrayed in segment II. In segment III, related bearer based and non-transporter based balance

procedures are exhibited and altered to suit the proposed topology. Area IV gives a correlation between the proposed topology and different topologies that are accessible for 5-level setup. In segment V, the reenactment aftereffect of a contextual analysis is exhibited to check the operation of the proposed topology for medium voltage application.

II. THE PROPOSED TOPOLOGY AND OPERATION

The proposed topology incorporates a dc-connection that is normal among the three stages. The dc-interface gives three voltage levels +2E, 0, and - 2E for the stage legs. Since every one of the stages have comparative arrangement, just a single stage leg of the proposed topology has been appeared in Fig. 1. Every one of the parts appeared in the figure have rise to working voltage E i.e. one fourth of the dc-connect voltage Vdc. The flying capacitors CA1 and CA2 are controlled to remain charged at the objective voltage E.

The accessible conditions of one stage leg are appeared in table I. To create level 2E, all the top arm switches SA1, SA2, SA3, SA4 ought to turn on. For level E, two decisions are accessible i.e. either through dc-connection's sure point (EP) or through dc-connection's nonpartisan point (E0). This repetition can be utilized to adjust the voltage of CA1. Level 0 is created through clasping the dc connection's unbiased indicate the yield (00). Negative states can be produced comparably because of the symmetry of the topology.

The operation of this topology is basically like topologies, for example, stacked multicell (SMC) converter where the positive and negative stacks work autonomously. Henceforth, the positive stack capacitor CA1 is utilized and adjusted amid the positive cycle and rest amid the negative cycle, while the negative stack capacitor CA2 is utilized and adjusted amid the negative cycle and rest amid the positive cycle. Thus, the flying capacitors will see the exchanging recurrence as opposed to line recurrence and in this manner the capacitor size is not very huge. Like the three-level NPC inverter, if the three periods of the heap are adjusted, the nonpartisan point voltage will be consistent in principle.

Notwithstanding, the voltage may marginally float away because of the lopsidedness in the components' spillage current. Furthermore, albeit little, there is constantly some awkwardness among the stages. A steady voltage float, despite the fact that little, can cause higher voltage crosswise over piece of the gadgets which can be deadly. By the by, this float can be repaid by infusing a little regular mode to the three stages. An essential element of the proposed topology is the even circulation of moves among exchanging gadgets. Consequently, exchanging misfortune which is the significant constraining element of inverter's warm execution is conveyed among the switches. As the principle result, the tradeoff between exchanging recurrence and current de rating is made strides. This gives the chance to either build the appraised current and energy of the inverter or increment the exchanging recurrence bringing about lower capacitor measure and enhanced voltage waveform quality.

III. MODULATION TECHNIQUES

Different adjustment strategies might be adjusted for the proposed topology. Bearer based regulation with sinusoidal or altered reference and in addition non-transporter based procedures for example, space vector adjustment and particular consonant disposal might be utilized to produce the door signals. The decision of a balance method is generally a tradeoff among the necessities of the application, unpredictability of the product, and cost of the control equipment.

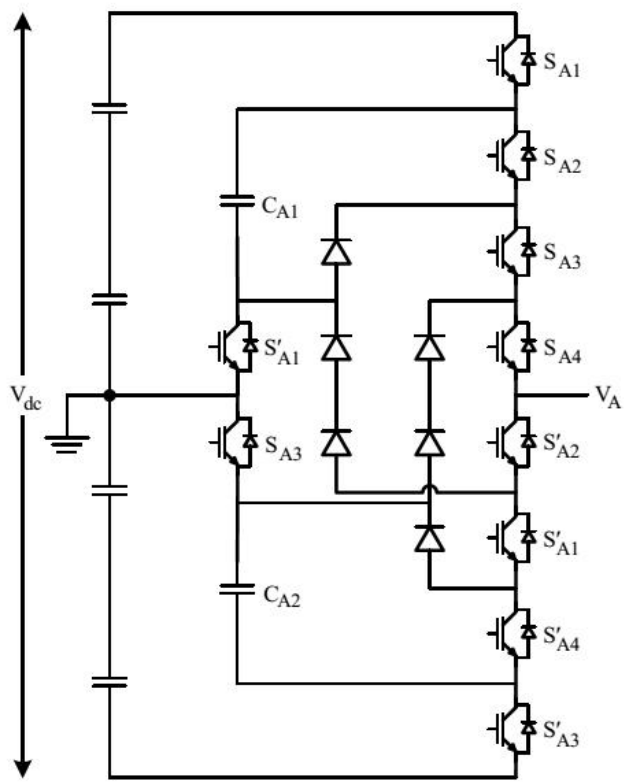


Fig. 1. A phase leg of the proposed 5-level hybrid topology

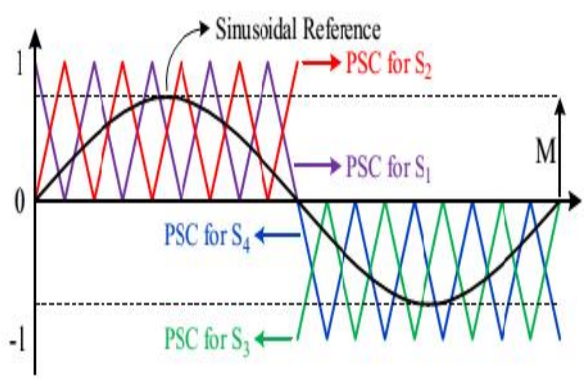
TABLE I.
SWITCHING STATES OF THE PROPOSED INVERTER

Level	State	S_1	S_2	S_3	S_4	C_1	C_2
+2E	+2E	1	1	1	1	N.A.	N.A.
+E	+EP	1	0	1	1	i>0 Charge i<0 Discharge	N.A.
	+E0	0	1	1	1	i>0 Discharge i<0 Charge	N.A.
0	0	0	0	1	1	N.A.	N.A.
-E	-E0	0	0	1	0	N.A.	i>0 Charge i<0 Discharge
	-EN	0	0	0	1	N.A.	i>0 Discharge i<0 Charge
-2E	-2E	0	0	0	0	N.A.	N.A.

S′1, S′2, S′3, S′4 are switched complementary to S1, S2, S3, S4 respectively. i>0 represents outbound current and i<0 represents inbound current. N.A. stands for Not Affected. For the 7-level topology +3E and -3E states increases and S5,S’5 switches&C3 capacitor increases.

A. Carrier-Based Modulation

Carrier set’s arrangement and reference waveform’s shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters. As for carrier set’s arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures. Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition PD are



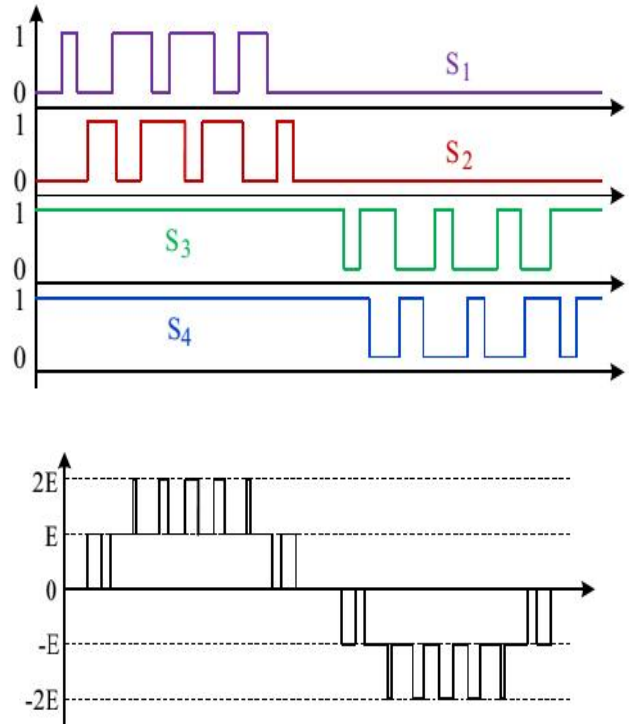


Fig. 2. Carrier- based modulation using PSC with sinusoidal reference for single phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

known to generate the best results for singe-phase and three phase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16]. The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to thepossibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control.

For the proposed inverter, a hybrid modulation technique is required due to the hybrid structure of the topology. Figure 3 illustrates the modulation technique for single-phase case. It is intuitive to separate the operation to positive and negative cycles, since each cycle is generated with a 3-level FC stack. The gate signals for each FC is then generated using PSC to provide natural voltage balancing for the flying capacitors. The generated output PWM waveform matches the APOD scheme.

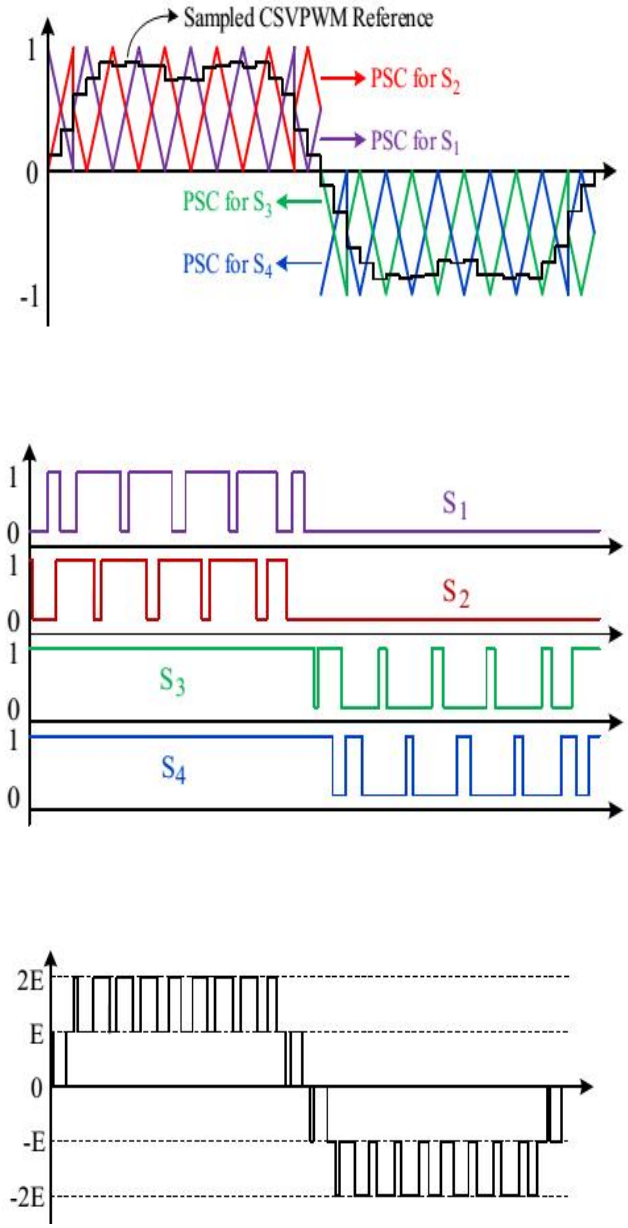


Fig. 3. Carrier-based modulation using modified PSC with sampled CSVPWM reference for three phase application. (a) Reference and carriers arrangement. (b) Gate signals. (c) Output waveform.

For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have π/2 phase shift compared to thenegative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by π/2 at the carrier band transitions. For thereference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulationtechnique using sampled CSVPWM along with modified PSC for the proposed inverter.

B. Non-Carrier-Based Modulation

For non-carrier-based modulation techniques such as SVM and SHE, the output PWM waveform may be generated first and then decomposed to the required switching signals. Figure 4 illustrates the required procedure to generate the gate signals for each phase leg. The 5-level PWM waveform is first separated to positive and negative cycle 3-level PWMs. Using state machine decoder, each cycle is then decomposed to two 2-level PWMs i.e. the required gate signals for each FC cell.

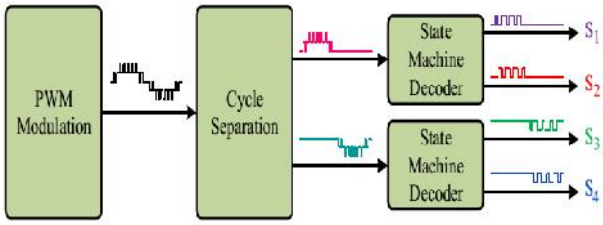


Fig. 4. Non-carrier-based modulation for a phase leg of the proposed inverter.

It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

IV. COMPARISON WITH OTHER TOPOLOGIES

A Comparison between the proposed topology and different 5-level topologies in terms of component count and loss distribution is listed in table II. The 5-level NPC has low switch count but the major problems are unbalanced operation of dc-link capacitors, poor loss distribution among switches, and excessive number of diodes. 5-Level FC provides low switch count and excellent loss distribution but requires high number of flying capacitors that can adversely affect the initial cost, maintenance and replacement surcharges, and reliability of the inverter. Capacitors' precharge requirement in some applications is also a drawback of this topology. The 5-level SMC topology provides lower capacitor count compared to FC and good loss distribution. However, high

switch count and high frequency switches in series are the main issues of this topology.

The 5-Level FC ANPC provides a good balance between the number of semiconductors and capacitors. The major issue with this topology is the poor loss distribution among the switches. The topology proposed in this paper, provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connectionof semiconductor devices, keep the balanced operation of dc link capacitors while keeping the number of costly components such as capacitors and switches as small as possible.

TABLE II. COMPARISON OF DIFFERENT TOPOLOGIES

Topology	Flying Capacitors	Switches	Diodes	Loss Distribution
5L-NPC	0	8	12	Poor
5L-FC	6	8	0	Excellent
5L-SMC	2	12	0	Good
5L-FC-ANPC	1	12	0	Fair
Proposed Topology	2	10	6	Good

The component counts in this table are per phase leg.

V. SIMULATION DESIGN AND RESULTS

To verify the operation of the proposed topology and the performance of the modulation techniques provided in section III, a model is developed and simulated with MATLAB software. The performance of the natural balancing technique for a three phase 12kV inverter supplying a 5MVA load at power factor of 0.7 is shown in Fig. 5. Centered space vector modulation (CSVPWM) is used at modulation index of 1.09

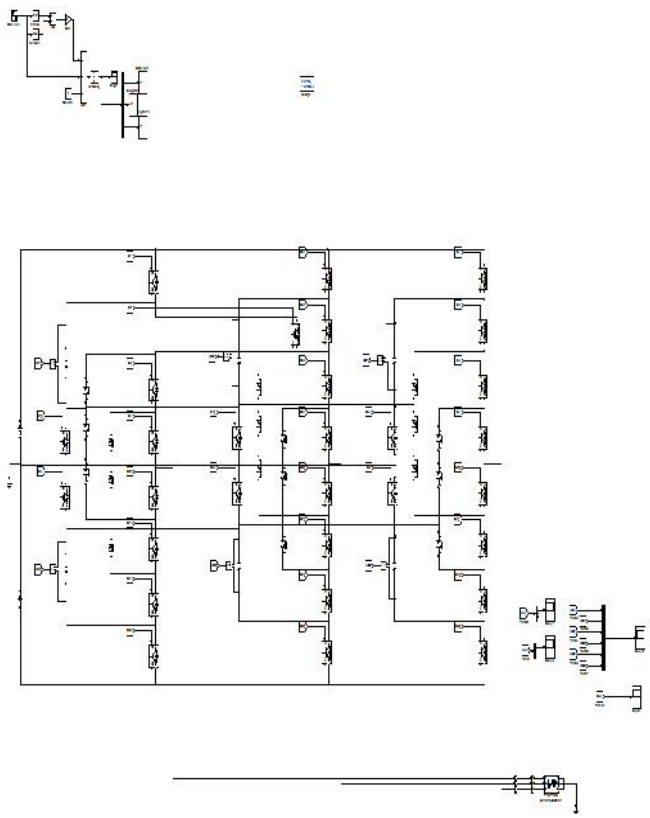


Fig5:SIMULATION BLOCK DIAGRAM OF 5-LEVEL INVERTER

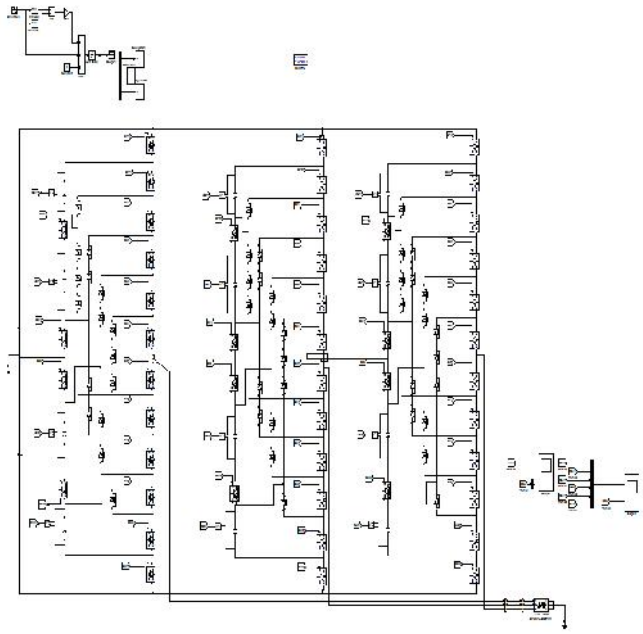


Fig6:SIMULATION BLOCK DIAGRAM OF 7-LEVEL INVERTER

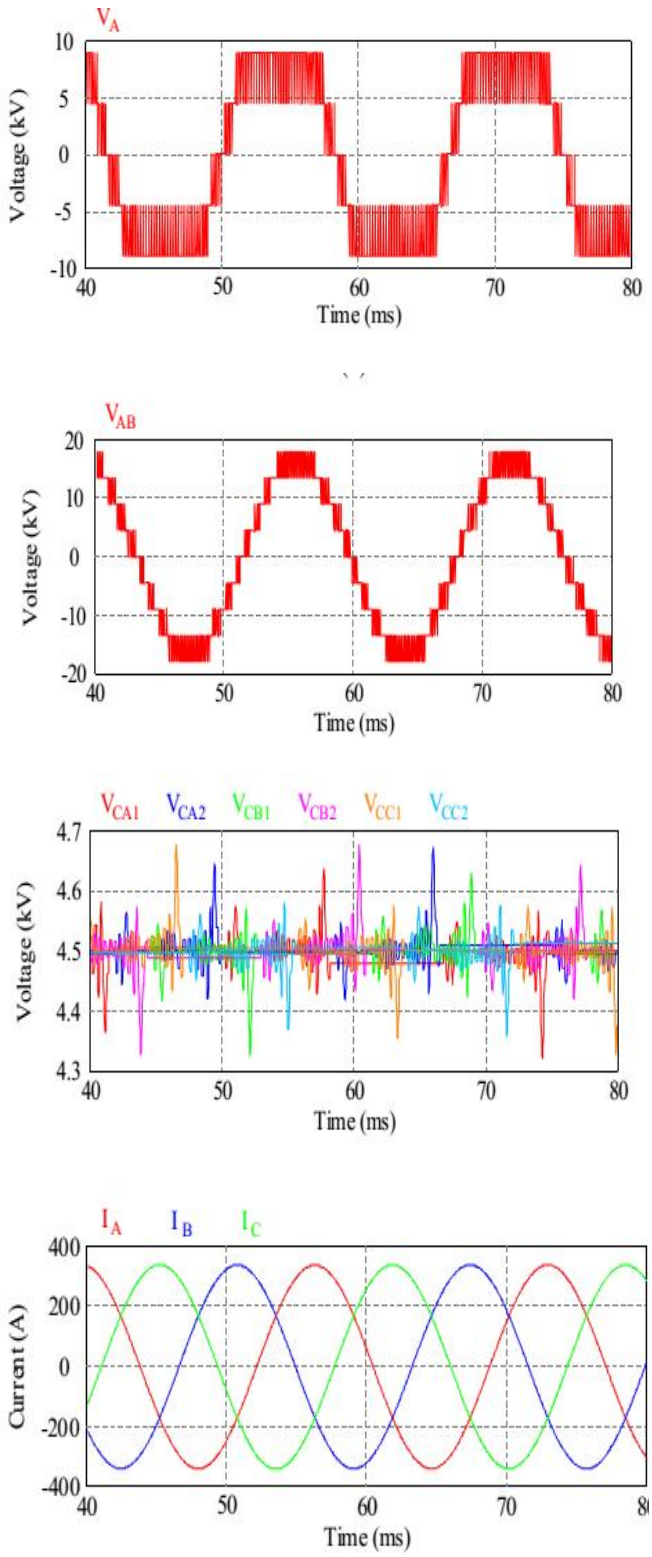


Fig. 8. Simulation results. (a) Phase voltage (b) Line voltage (c) Flying capacitor voltages (d) Load current frequency 5kHz. The dc-link voltage is set at 18kV and flying capacitors are 330µF. It can be seen that even without an RLC balance booster, the capacitor voltage errors are limited to less than 4%.

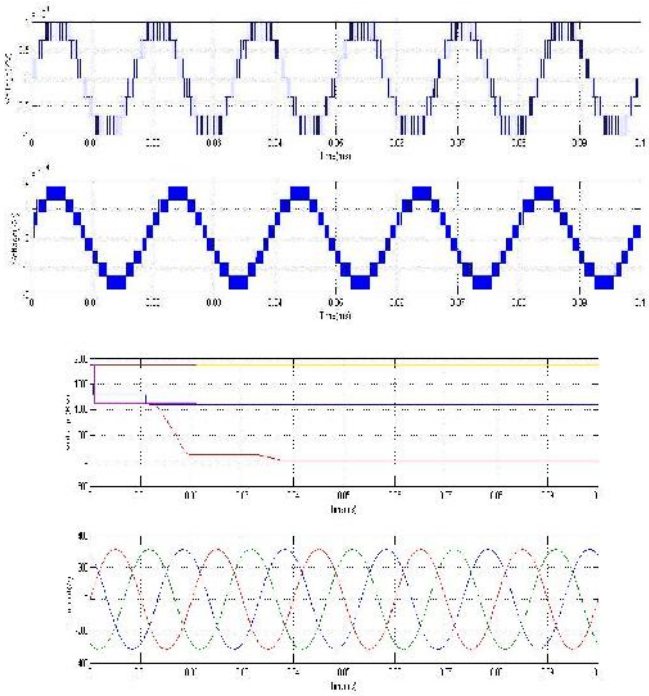


Fig. 9: Simulation results. (a) Phase voltage (b) Line voltage (c) Flying capacitor voltages (d) Load current frequency 5kHz

VI. CONCLUSION

A new hybrid 7-level inverter topology and modulation technique is proposed. Compared to 5-level ANPC as the most similar topology, this new topology requires two less switches at the cost of an additional capacitor and six diodes. Similarly7-level proposed inverter also requires less number of components compared to other multilevel inverter topologies. However, since the capacitors still see the switching frequency and their size remain the same, it is expected to reduce the inverter's total cost. Also, unlike 7-level ANPC, all switches must withstand the same voltage which eliminates the need for series connection of switches and associated simultaneous turn on and off problem. Good loss distribution among switches can increase the inverters rated power or provide higher switching frequency and smaller capacitor size. Simulation results verify through **MATLAB/SIMULINK** environment.

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